

August 1997

## +5V Powered, Dual RS-232 Transmitter/Receiver

### Features

- Meets All RS-232C and V.28 Specifications
- Requires Only Single +5V Power Supply
- Onboard Voltage Doubler/Inverter
- Low Power Consumption
- 2 Drivers
  - $\pm 9V$  Output Swing for +5V Input
  - $300\Omega$  Power-off Source Impedance
  - Output Current Limiting
  - TTL/CMOS Compatible
  - $30V/\mu s$  Maximum Slew Rate
- 2 Receivers
  - $\pm 30V$  Input Voltage Range
  - $3k\Omega$  to  $7k\Omega$  Input Impedance
  - 0.5V Hysteresis to Improve Noise Rejection
- All Critical Parameters are Guaranteed Over the Entire Commercial, Industrial and Military Temperature Ranges

### Applications

- Any System Requiring RS-232 Communications Port
  - Computer - Portable and Mainframe
  - Peripheral - Printers and Terminals
  - Portable Instrumentation
  - Modems
- Dataloggers

### Description

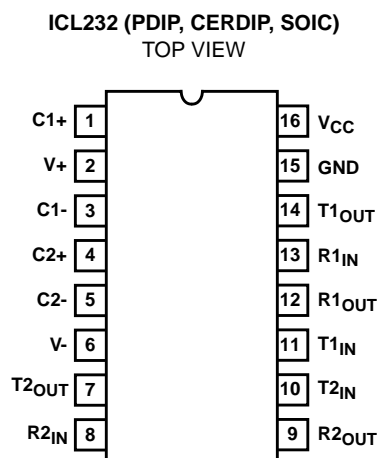
The ICL232 is a dual RS-232 transmitter/receiver interface circuit that meets all EIA RS-232C and V.28 specifications. It requires a single +5V power supply, and features two onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply.

The drivers feature true TTL/CMOS input compatibility, slew-rate-limited output, and  $300\Omega$  power-off source impedance. The receivers can handle up to  $\pm 30V$ , and have a  $3k\Omega$  to  $7k\Omega$  input impedance. The receivers also have hysteresis to improve noise rejection.

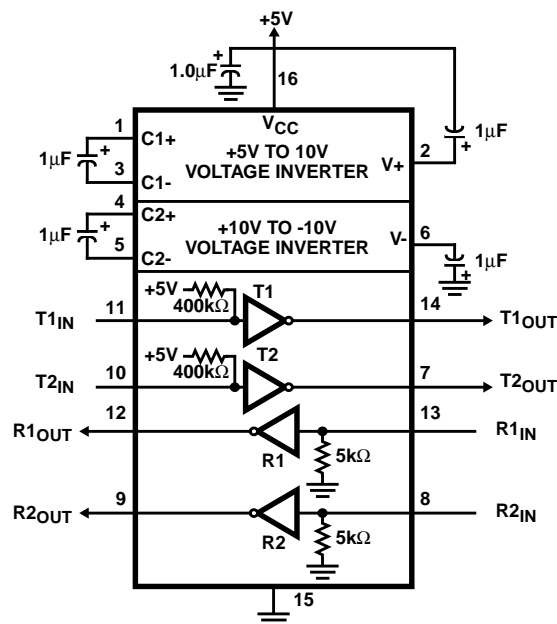
### Ordering Information

PART NUMBER	TEMP. RANGE ( $^{\circ}C$ )	PACKAGE	PKG. NO.
ICL232CPE	0 to 70	16 Ld PDIP	E16.3
ICL232CBE	0 to 70	16 Ld SOIC	M16.3
ICL232IPE	-40 to 85	16 Ld PDIP	E16.3
ICL232IJE	-40 to 85	16 Ld Cerdip	F16.3
ICL232IBE	-40 to 85	16 Ld SOIC	M16.3
ICL232MJE	-55 to 125	16 Ld Cerdip	F16.3

### Pinout



### Functional Diagram



## Absolute Maximum Ratings

$V_{CC}$ to Ground	$(GND - 0.3V) < V_{CC} < 6V$
$V+$ to Ground	$(V_{CC} - 0.3V) < V+ < 12V$
$V-$ to Ground	$-12V < V- < (GND + 0.3V)$
Input Voltages	
$T1_{IN}, T2_{IN}$	$(V- - 0.3V) < V_{IN} < (V+ + 0.3V)$
$R1_{IN}, R2_{IN}$	$\pm 30V$
Output Voltages	
$T1_{OUT}, T2_{OUT}$	$(V- - 0.3V) < V_{TXOUT} < (V+ + 0.3V)$
$R1_{OUT}, R2_{OUT}$	$(GND - 0.3V) < V_{RXOUT} < (V_{CC} + 0.3V)$
Short Circuit Duration	
$T1_{OUT}, T2_{OUT}$	Continuous
$R1_{OUT}, R2_{OUT}$	Continuous

## Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ ( $^{\circ}C/W$ )	$\theta_{JC}$ ( $^{\circ}C/W$ )
CERDIP Package	80	18
PDIP Package	100	N/A
SOIC Package	100	N/A
Maximum Junction Temperature		
Plastic Packages		150 $^{\circ}C$
Ceramic Package		175 $^{\circ}C$
Maximum Storage Temperature Range		-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)		300 $^{\circ}C$

## Operating Conditions

Temperature Ranges	
ICL232C	0 $^{\circ}C$ to 70 $^{\circ}C$
ICL232I	-40 $^{\circ}C$ to 85 $^{\circ}C$
ICL232M	-55 $^{\circ}C$ to 125 $^{\circ}C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications

Test Conditions:  $V_{CC} = +5V \pm 10\%$ ,  $T_A$  = Operating Temperature Range. Test Circuit as in Figure 8 Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Transmitter Output Voltage Swing, $T_{OUT}$	$T1_{OUT}$ and $T2_{OUT}$ Loaded with 3k $\Omega$ to Ground	$\pm 5$	$\pm 9$	$\pm 10$	V
Power Supply Current, $I_{CC}$	Outputs Unloaded, $T_A = 25^{\circ}C$	-	5	10	mA
$T1_{IN}$ , Input Logic Low, $V_{IL}$		-	-	0.8	V
$T1_{IN}$ , Input Logic High, $V_{IH}$		2.0	-	-	V
Logic Pullup Current, $I_P$	$T1_{IN}, T2_{IN} = 0V$	-	15	200	$\mu A$
RS-232 Input Voltage Range, $V_{IN}$		-30	-	+30	V
Receiver Input Impedance, $R_{IN}$	$V_{IN} = \pm 3V$	3.0	5.0	7.0	k $\Omega$
Receiver Input Low Threshold, $V_{IN}$ (H-L)	$V_{CC} = 5V, T_A = 25^{\circ}C$	0.8	1.2	-	V
Receiver Input High Threshold, $V_{IN}$ (L-H)	$V_{CC} = 5V, T_A = 25^{\circ}C$	-	1.7	2.4	V
Receiver Input Hysteresis, $V_{HYST}$		0.2	0.5	1.0	V
TTL/CMOS Receiver Output Voltage Low, $V_{OL}$	$I_{OUT} = 3.2mA$	-	0.1	0.4	V
TTL/CMOS Receiver Output Voltage High, $V_{OH}$	$I_{OUT} = -1.0mA$	3.5	4.6	-	V
Propagation Delay, $t_{PD}$	RS-232 to TTL	-	0.5	-	$\mu s$
Instantaneous Slew Rate, SR	$C_L = 10pF, R_L = 3k\Omega, T_A = 25^{\circ}C$ (Notes 2, 3)	-	-	30	V/ $\mu s$
Transition Region Slew Rate, $SR_T$	$R_L = 3k\Omega, C_L = 2500pF$ Measured from +3V to -3V or -3V to +3V	-	3	-	V/ $\mu s$
Output Resistance, $R_{OUT}$	$V_{CC} = V+ = V- = 0V, V_{OUT} = \pm 2V$	300	-	-	$\Omega$
RS-232 Output Short Circuit Current, $I_{SC}$	$T1_{OUT}$ or $T2_{OUT}$ Shorted to GND	-	$\pm 10$	-	mA

### NOTES:

2. Guaranteed by design.
3. See Figure 4 for definition.

## Test Circuits

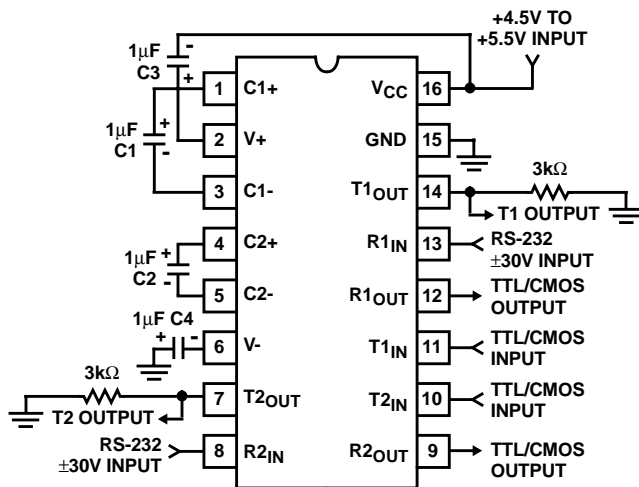


FIGURE 1. GENERAL TEST CIRCUIT

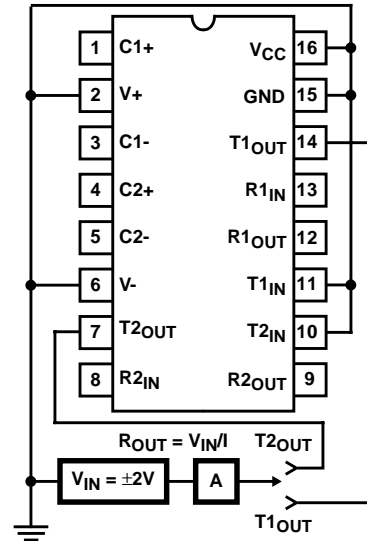


FIGURE 2. POWER-OFF SOURCE RESISTANCE CONFIGURATION

## Typical Performance Curves

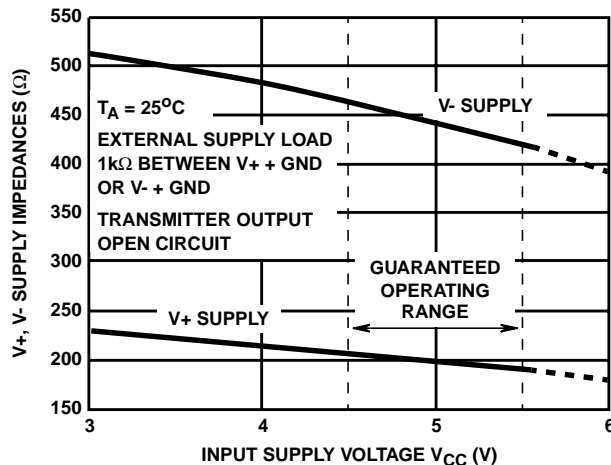
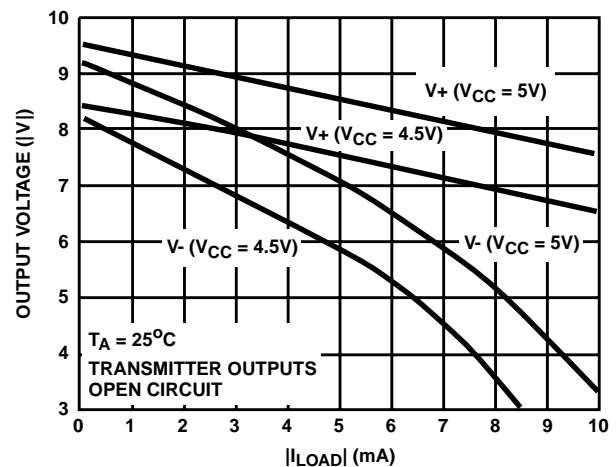
FIGURE 3. V+, V- OUTPUT IMPEDANCES vs  $V_{CC}$ 

FIGURE 4. V+, V- OUTPUT VOLTAGES vs LOAD CURRENT

## Pin Descriptions

PDIP, Cerdip	SOIC	PIN NAME	DESCRIPTION
1	1	C1+	External capacitor "+" for internal voltage doubler.
2	2	V+	Internally generated +10V (typical) supply.
3	3	C1-	External capacitor "-" for internal voltage doubler.
4	4	C2+	External capacitor "+" internal voltage inverter.
5	5	C2-	External capacitor "-" internal voltage inverter.
6	6	V-	Internally generated -10V (typical) supply.
7	7	T2OUT	RS-232 Transmitter 2 output $\pm 10V$ (typical).
8	8	R2IN	RS-232 Receiver 2 input, with internal 5K pulldown resistor to GND.
9	9	R2out	Receiver 2 TTL/CMOS output.
10	10	T2IN	Transmitter 2 TTL/CMOS input, with internal 400K pullup resistor to $V_{CC}$ .
11	11	T1IN	Transmitter 1 TTL/CMOS input, with internal 400K pullup resistor to $V_{CC}$ .

# Pin Descriptions (Continued)

PDIP, Cerdip	SOIC	PIN NAME	DESCRIPTION
12	12	R1 <sub>OUT</sub>	Receiver 1 TTL/CMOS output.
13	13	R1 <sub>IN</sub>	RS-232 Receiver 1 input, with internal 5K pulldown resistor to GND.
14	14	T1 <sub>OUT</sub>	RS-232 Transmitter 1 output $\pm 10V$ (typical).
15	15	GND	Supply Ground.
16	16	V <sub>CC</sub>	Positive Power Supply +5V $\pm 10\%$

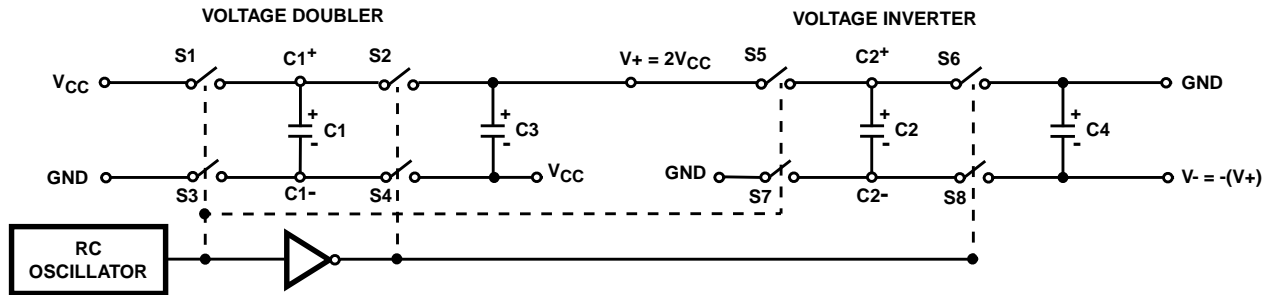


FIGURE 5. DUAL CHARGE PUMP

## Detailed Description

The ICL232 is a dual RS-232 transmitter/receiver powered by a single +5V power supply which meets all EIA RS232C specifications and features low power consumption. The functional diagram illustrates the major elements of the ICL232. The circuit is divided into three sections: a voltage doubler/inverter, dual transmitters, and dual receivers Voltage Converter.

An equivalent circuit of the dual charge pump is illustrated in Figure 5.

The voltage quadrupler contains two charge pumps which use two phases of an internally generated clock to generate +10V and -10V. The nominal clock frequency is 16kHz. During phase one of the clock, capacitor C1 is charged to V<sub>CC</sub>. During phase two, the voltage on C1 is added to V<sub>CC</sub>, producing a signal across C2 equal to twice V<sub>CC</sub>. At the same time, C3 is also charged to 2V<sub>CC</sub>, and then during phase one, it is inverted with respect to ground to produce a signal across C4 equal to -2V<sub>CC</sub>. The voltage converter accepts input voltages up to 5.5V. The output impedance of the doubler (V+) is approximately 200Ω, and the output impedance of the inverter (V-) is approximately 450Ω. Typical graphs are presented which show the voltage converters output vs input voltage and output voltages vs load characteristics. The test circuit (Figure 3) uses 1μF capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, and increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the V+ and V- supplies.

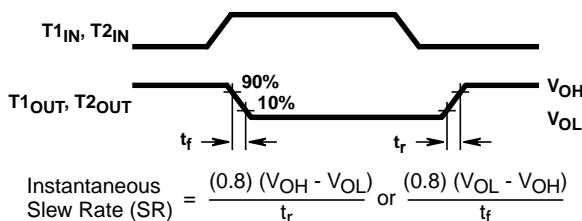


FIGURE 6. SLEW RATE DEFINITION

## Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V<sub>CC</sub>, or 1.3V for V<sub>CC</sub> = 5V. A logic 1 at the input results in a voltage of between -5V and V- at the output, and a logic 0 results in a voltage between +5V and (V+ - 0.6V). Each transmitter input has an internal 400kΩ pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specification of  $\pm 5V$  minimum with the worst case conditions of: both transmitters driving 3kΩ minimum load impedance, V<sub>CC</sub> = 4.5V, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/μs. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300Ω with  $\pm 2V$  applied to the outputs and V<sub>CC</sub> = 0V.

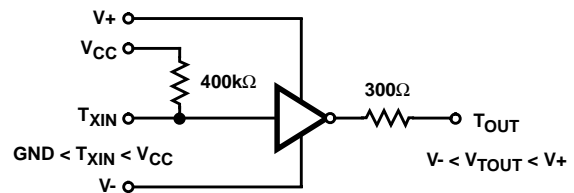


FIGURE 7. TRANSMITTER

## Receivers

The receiver inputs accept up to  $\pm 30V$  while presenting the required 3kΩ to 7kΩ input impedance even if the power is off (V<sub>CC</sub> = 0V). The receivers have a typical input threshold of 1.3V which is within the  $\pm 3V$  limits, known as the transition region, of the RS-232 specification. The receiver output is 0V to V<sub>CC</sub>. The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis to improve noise rejection.

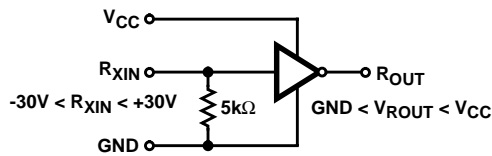
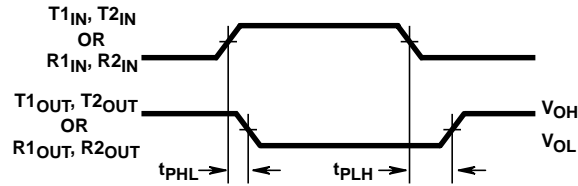


FIGURE 8. RECEIVER



$$\text{Average Propagation Delay} = \frac{t_{PHL} + t_{PLH}}{2}$$

FIGURE 9. PROPAGATION DELAY DEFINITION

## Applications

The ICL232 may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where  $\pm 12V$  power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 10. Fixed output signals such as DTR (data terminal ready) and DSRS (data signaling rate select)

is generated by driving them through a  $5k\Omega$  resistor connected to  $V_+$ .

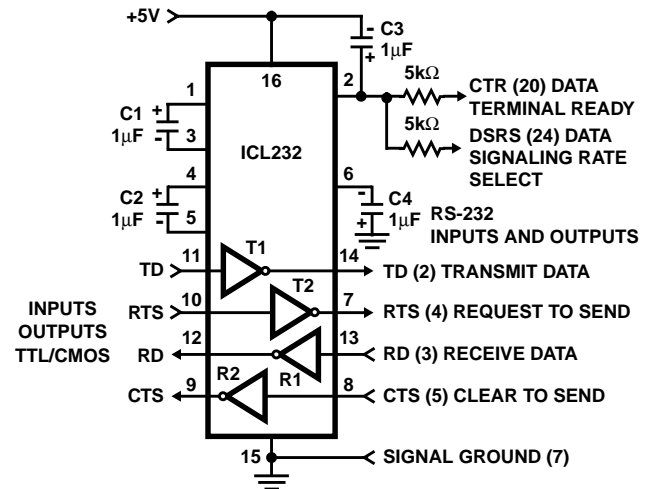


FIGURE 10. SIMPLE DUPLEX RS-232 PORT WITH CTS/RTS HANDSHAKING

In applications requiring four RS-232 inputs and outputs (Figure 11), note that each circuit requires two charge pump capacitors ( $C1$  and  $C2$ ) but can share common reservoir capacitors ( $C3$  and  $C4$ ). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.

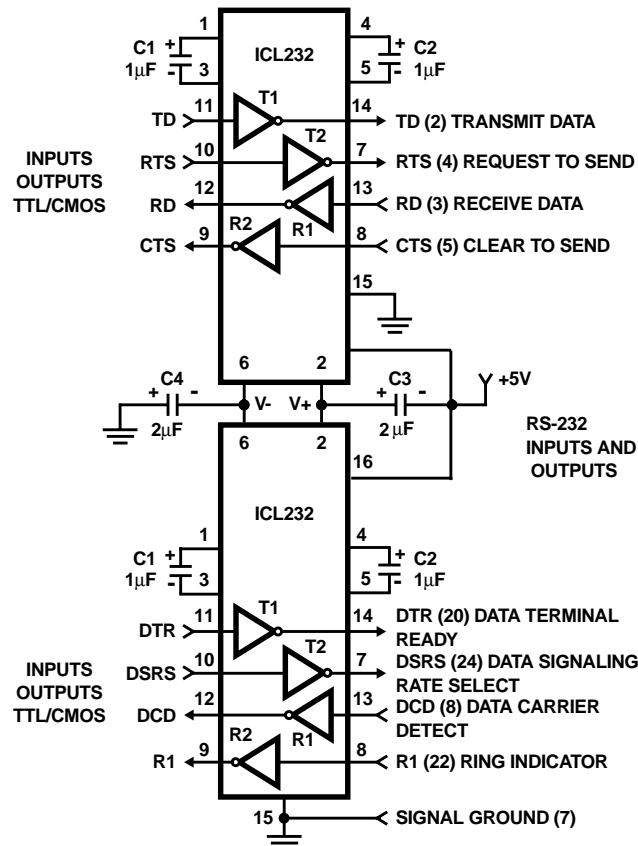


FIGURE 11. COMBINING TWO ICL232s FOR 4 PAIRS OF RS-232 INPUTS AND OUTPUTS