Quad SPST CMOS Analog Switches

FEATURES

- Low On-Resistance: 50 Ω
- Low Leakage: 80 pA
- Low Power Consumption: 22 nW
- Fast Switching Action—t_{ON}: 120 ns
- Low Charge Injection
- DG211/DG212 Upgrades
- TTL/CMOS Logic Compatible

BENEFITS

- Low Signal Errors and Distortion
- Reduced Power Supply Requirements
- Faster Throughput
- Improved Reliability
- Reduced Pedestal Errors
- Simple Interfacing

APPLICATIONS

- Audio Switching
- Battery Powered Systems
- Data Acquisition
- Sample-and-Hold Circuits
- Telecommunication Systems
- Automatic Test Equipment
- Single Supply Circuits
- Hard Disk Drives

DESCRIPTION

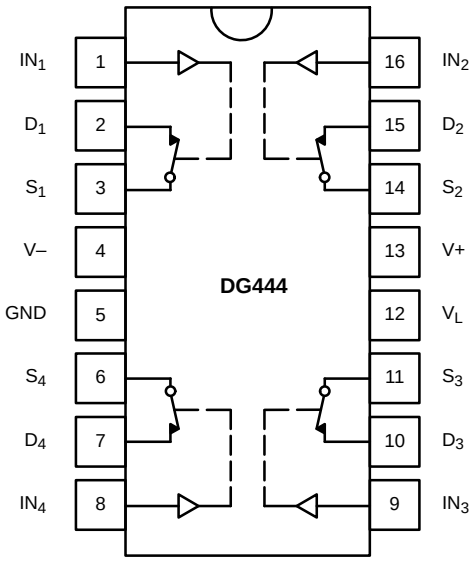
The DG444/DG445 monolithic quad analog switches are designed to provide high speed, low error switching of analog signals. The DG444 has a normally closed function. The DG445 has a normally open function. Combining low power (22 nW, typ) with high speed (t_{ON}: 120 ns, typ), the DG444/DG445 are ideally suited for upgrading DG211/212 sockets. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

To achieve high-voltage ratings and superior switching performance, the DG444/DG445 are built on Vishay Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages to the supply levels when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

Dual-In-Line and SOIC



Top View

TRUTH TABLE		
Logic	**DG444**	**DG445**
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
–40°C to 85°C	16-Pin Plastic DIP	DG444DJ
		DG445DJ
	16-Pin Narrow SOIC	DG444DY
		DG445DY

ABSOLUTE MAXIMUM RATINGS

V+ to V– ..... 44 V
GND to V– ..... 25 V
V_L ..... (GND –0.3 V) to (V+) + 0.3 V
Digital Inputs[a] V_S, V_D ..... (V–) –2 V to (V+) +2 V
or 30 mA, whichever occurs first
Continuous Current (Any Terminal) ..... 30 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle) ..... 100 mA
Storage Temperature ..... –65 to 125°C

Power Dissipation (Package)b
16-Pin Plastic DIP[c] ..... 450 mW
16-Pin Narrow Body SOIC[d] ..... 640 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C
d. Derate 8 mW/°C above 75°C

SPECIFICATIONS FOR DUAL SUPPLIES

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]		Temp[a]	D Suffix –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch								
Analog Signal Range[d]	V_{ANALOG}			Full	–15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = –10 mA, V_D = ±8.5 V V+ = 13.5 V, V– = –13.5 V		Room Full		50	85 100	Ω
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5, V– = –16.5 V V_D = ±15.5 V, V_S = ∓15.5 V		Room Full	–0.5 –5	±0.01	0.5 5	nA
	$I_{D(off)}$			Room Full	–0.5 –5	±0.01	0.5 5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 16.5 V, V– = –16.5 V V_S = V_D = ±15.5 V		Room Full	–0.5 –10	±0.08	0.5 10	
Digital Control								
Input Current V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V All Other = 2.4 V		Full	–500	–0.01	500	nA
Input Current V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V All Other = 0.8 V		Full	–500	0.01	500	
Dynamic Characteristics								
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF V_S = ±10 V, See Figure 2		Room		120	250	ns
Turn-Off Time	t_{OFF}		DG444	Room		110	140	
			DG445	Room		160	210	
Charge Injection[e]	Q	C_L = 1 nF, V_S = 0 V V_{gen} = 0 V, R_{gen} = 0 Ω		Room		–1		pC
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		Room		60		dB
Crosstalk (Channel-to-Channel)[d]	X_{TALK}			Room		100		
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz		Room		4		pF
Drain Off Capacitance	$C_{D(off)}$			Room		4		
Channel On Capacitance	$C_{D(on)}$	V_{ANALOG} = 0 V		Room		16		
Power Supplies								
Positive Supply Current	I+	V+ = 16.5 V, V– = –16.5 V V_{IN} = 0 or 5 V		Room Full		0.001	1 5	µA
Negative Supply Current	I–			Room Full	–1 –5	–0.0001		
Logic Supply Current	I_L			Room Full		0.001	1 5	
Ground Current	I_{GND}			Room Full	–1 –5	–0.001		

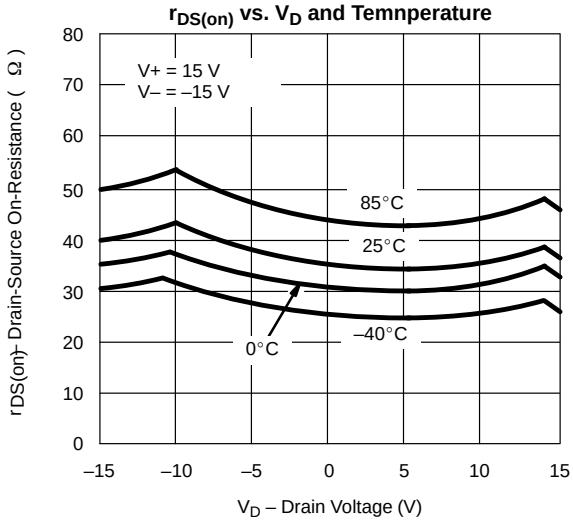
SPECIFICATIONS FOR UNIPOLAR SUPPLIES

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V– = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	Temp[a]	D Suffix –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	0		12	V
Drain-Source On-Resistance[d]	$r_{DS(on)}$	I_S = –10 mA, V_D = 3 V, 8 V V+ = 10.8 V, V_L = 5.25 V	Room Full		100	160 200	Ω
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, V_S = 8 V See Figure 2	Room		300	450	ns
Turn-Off Time	t_{OFF}		Room		60	200	
Charge Injection	Q	C_L = 1 nF, V_{gen} = 6 V, R_{gen} = 0 Ω	Room		2		pC
Power Supplies							
Positive Supply Current	I+	V+ = 13.2 V, V_{IN} = 0 or 5 V	Room Full		0.001	1 5	µA
Negative Supply Current	I–	V_{IN} = 0 or 5 V	Room Full	–1 –5	–0.0001		
Logic Supply Current	I_L	V_L = 5.25 V, V_{IN} = 0 or 5 V	Room Full		0.001	1 5	
Ground Current	I_{GND}	V_{IN} = 0 or 5 V	Room Full	–1 –5	–0.001		

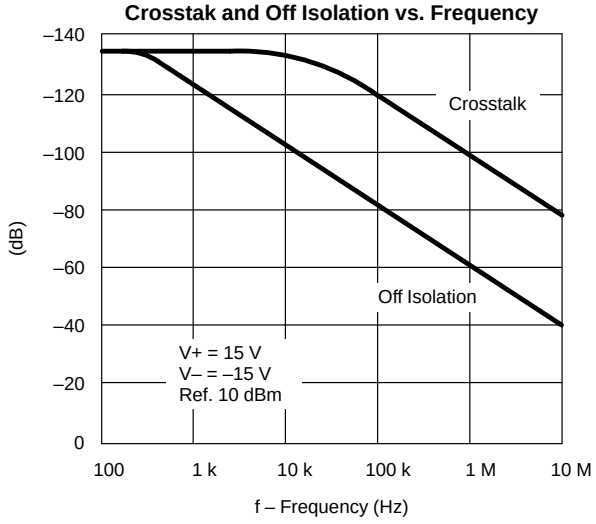
Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

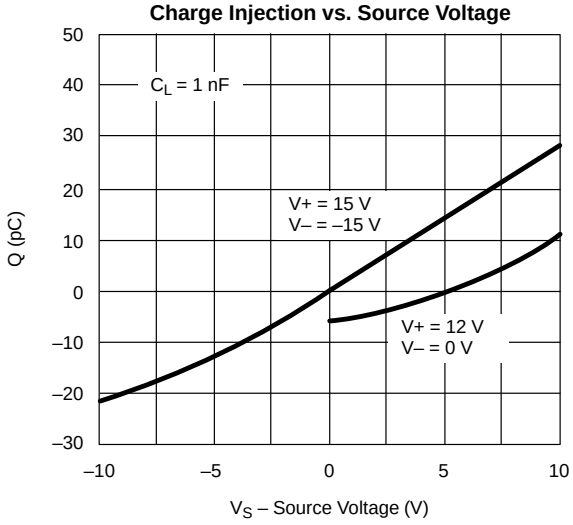
$r_{DS(on)}$ vs. V_D and Temnperature



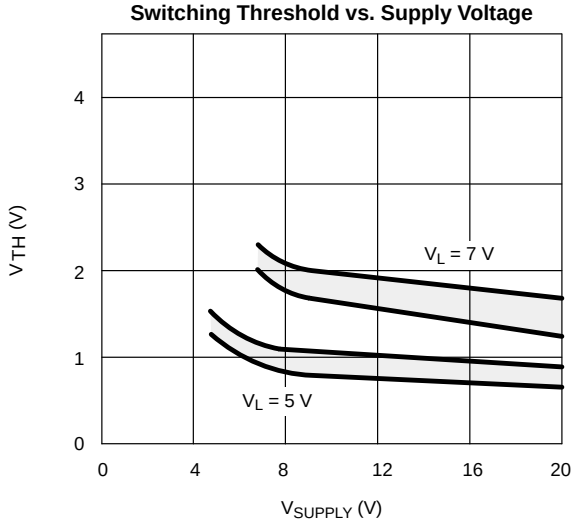
Crosstak and Off Isolation vs. Frequency



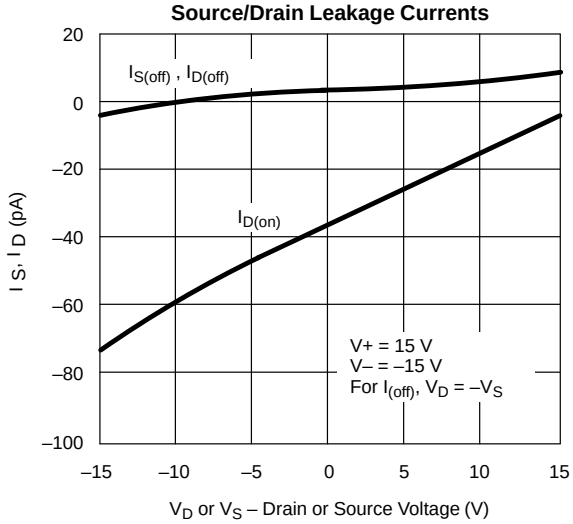
Charge Injection vs. Source Voltage



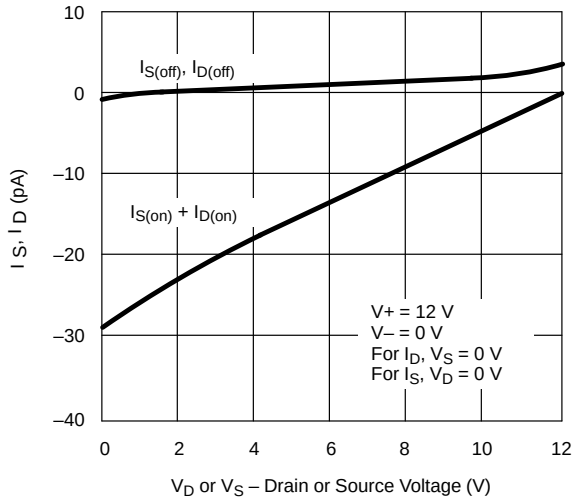
Switching Threshold vs. Supply Voltage



Source/Drain Leakage Currents

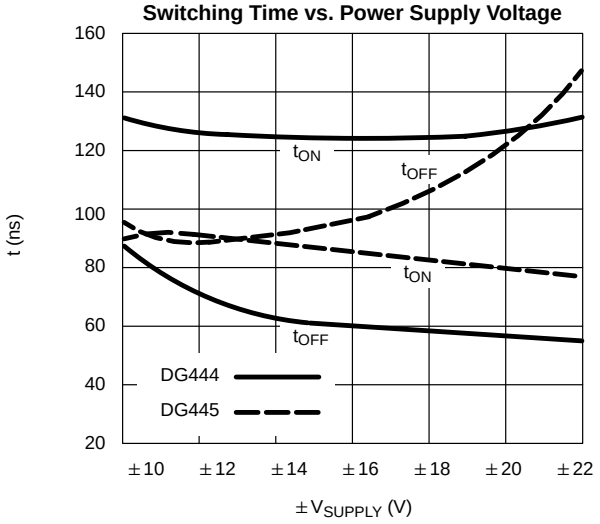


Source/Drain Leakage Currents (Single 12-V Supply)

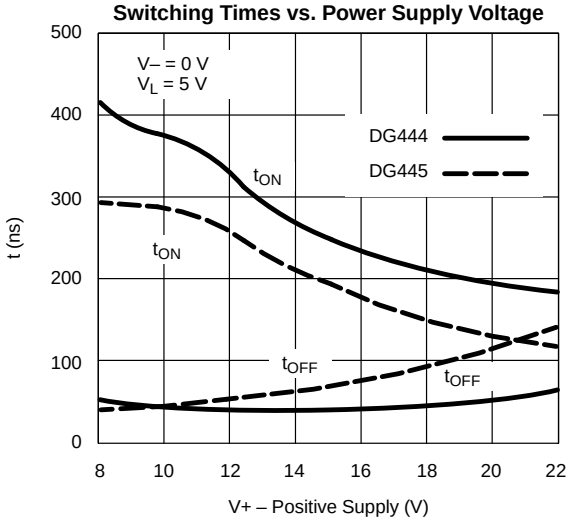


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

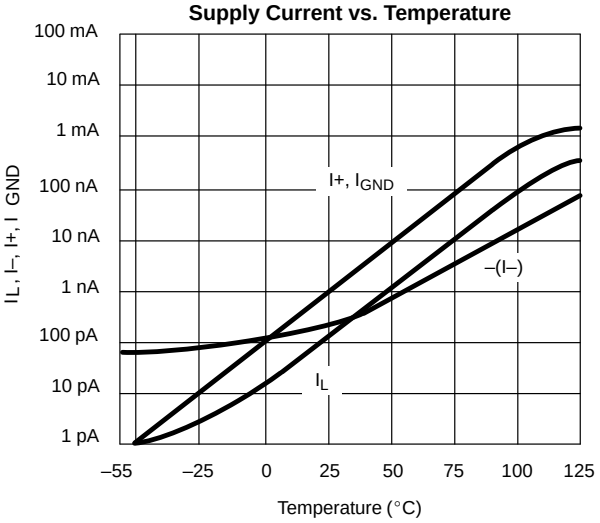
Switching Time vs. Power Supply Voltage



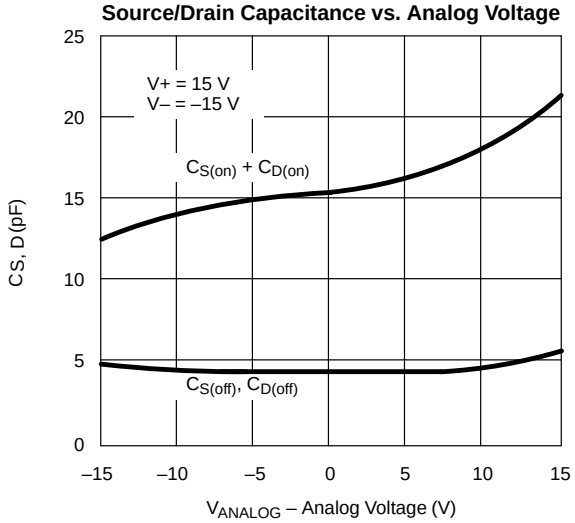
Switching Times vs. Power Supply Voltage



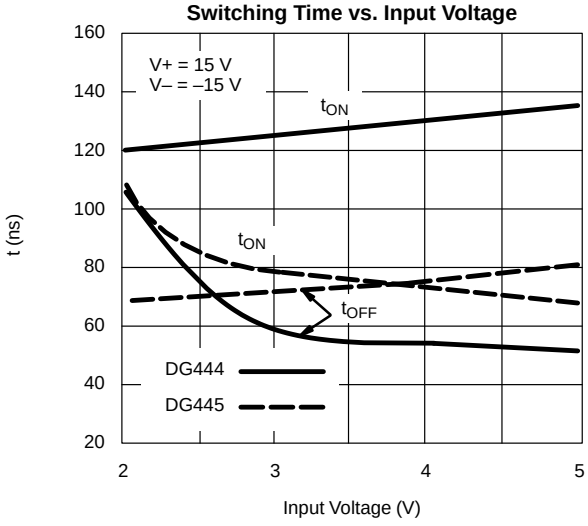
Supply Current vs. Temperature



Source/Drain Capacitance vs. Analog Voltage



Switching Time vs. Input Voltage



SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

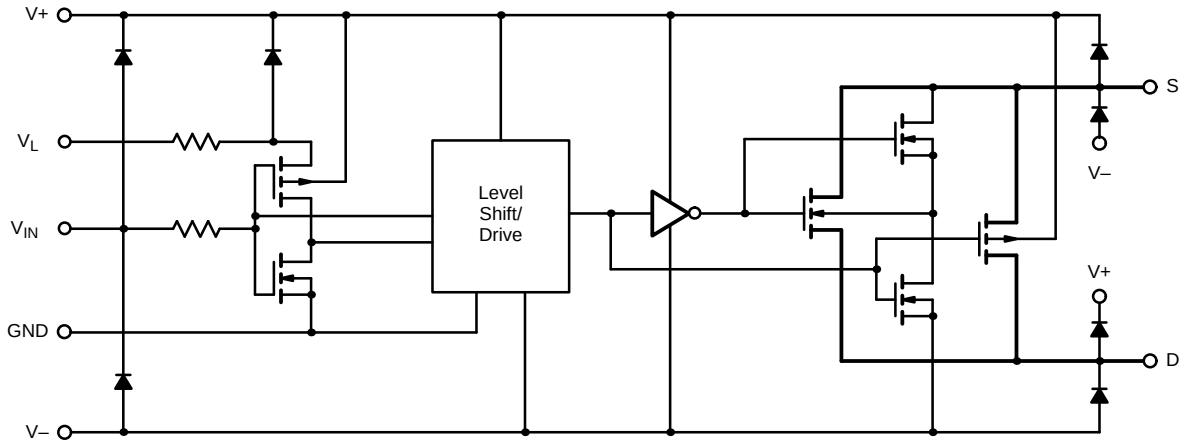
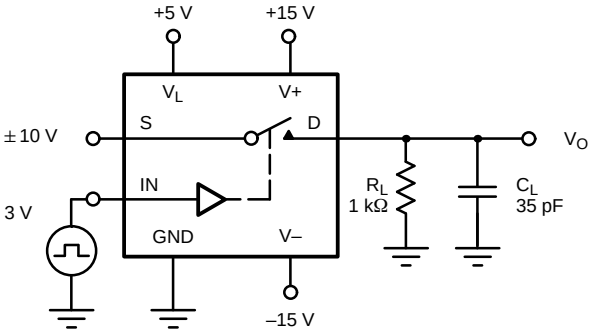
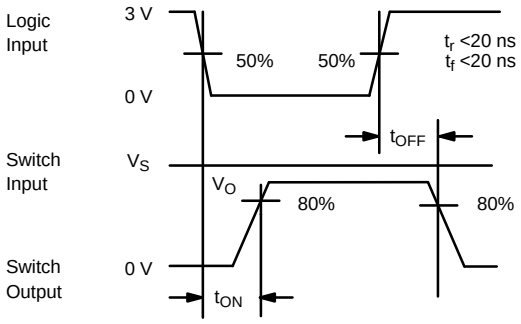


FIGURE 1.

TEST CIRCUITS

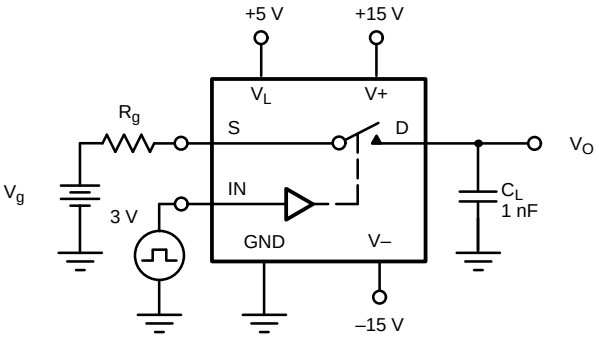


C_L (includes fixture and stray capacitance)



Note: Logic input waveform is inverted for DG445.

FIGURE 2. Switching Time



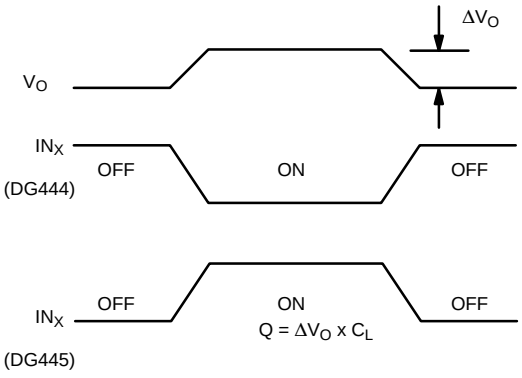


FIGURE 3. Charge Injection

TEST CIRCUITS

C = 1 mF tantalum in parallel with 0.01 mF ceramic

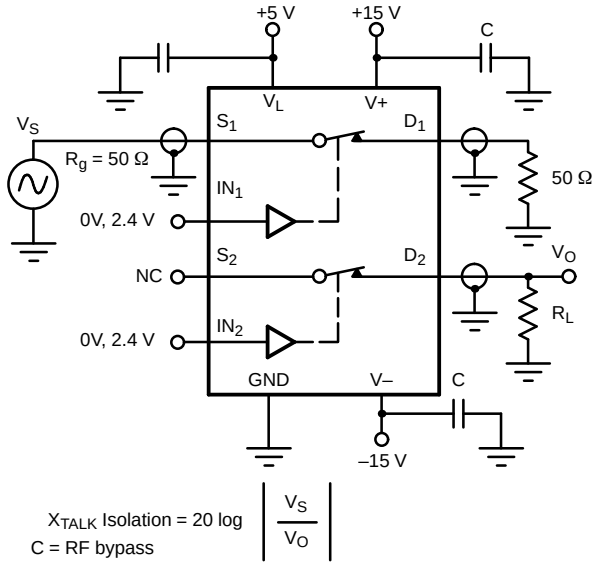


FIGURE 4. Crosstalk

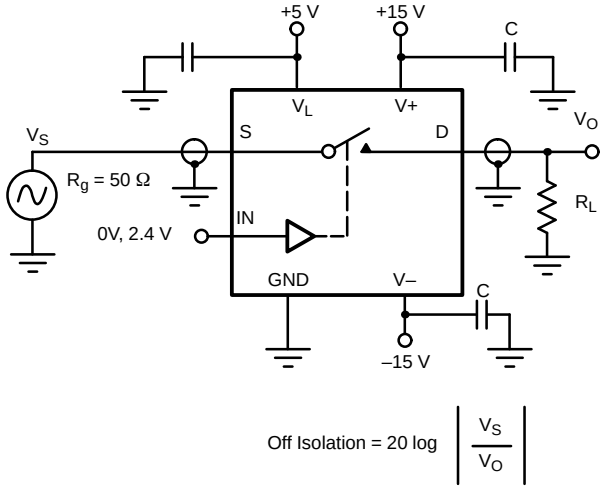


FIGURE 5. Off Isolation

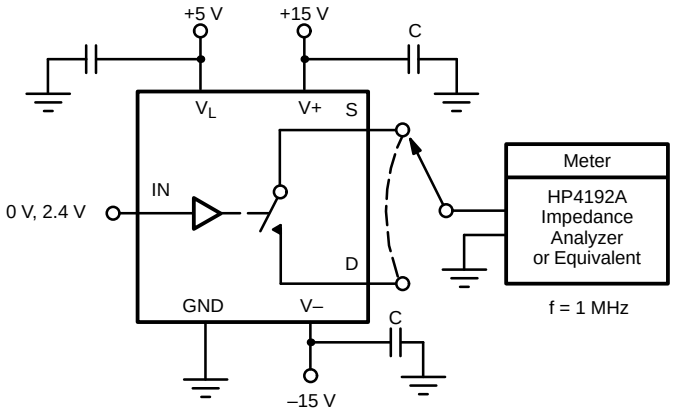


FIGURE 6. Source/Drain Capacitances

APPLICATIONS

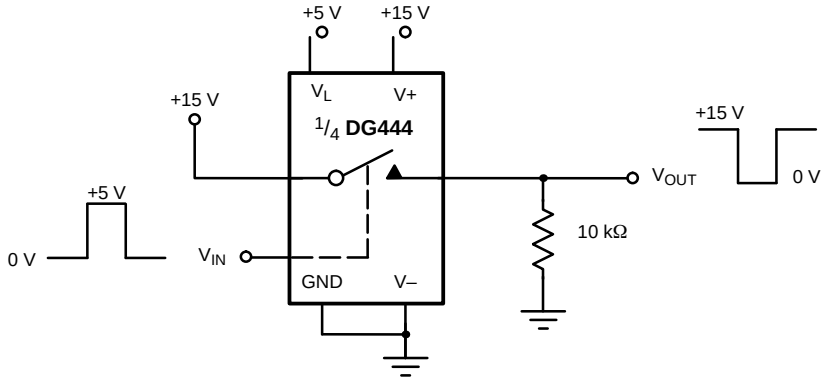


FIGURE 7. Level Shifter

APPLICATIONS

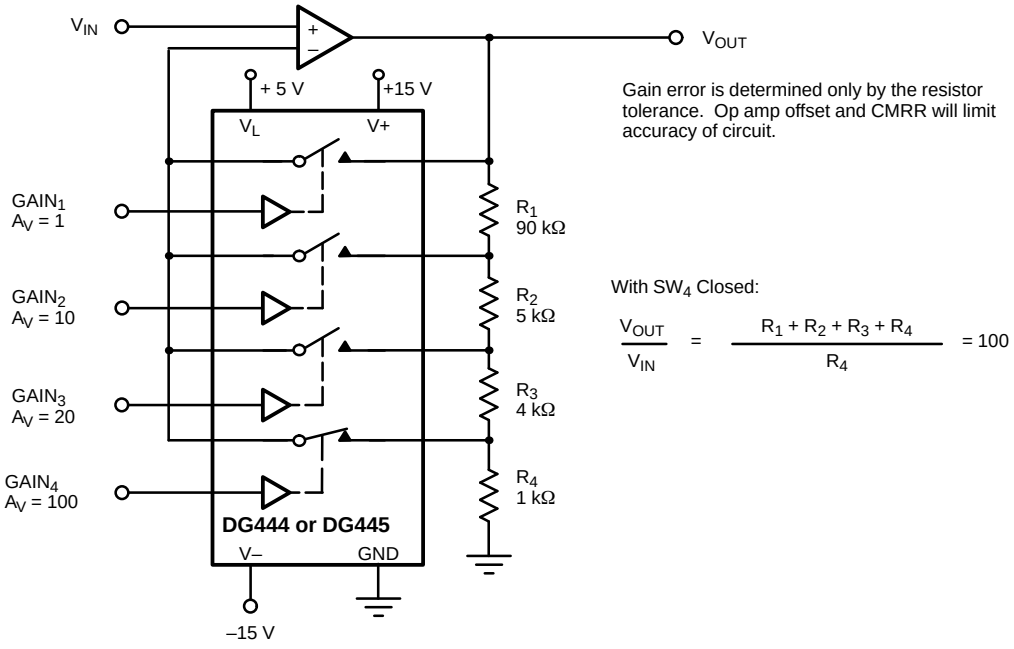


FIGURE 8. Precision-Weighted Resistor Programmable-Gain Amplifier

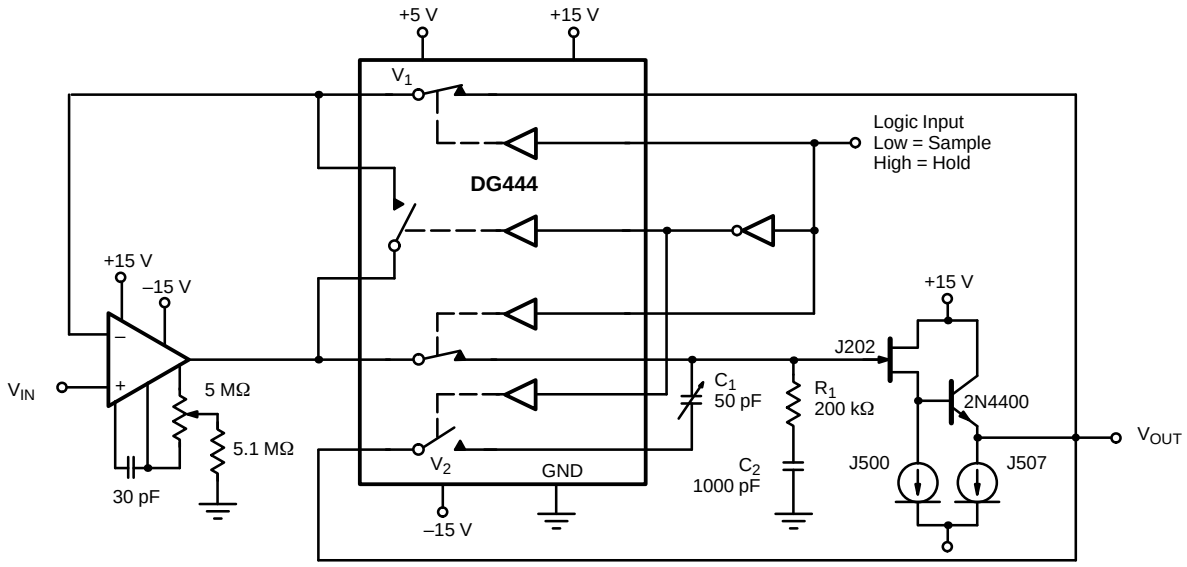


FIGURE 9. Precision Sample-and-Hold

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