

**SN55451B, SN55452B, SN55453B, SN55454B
SN75451B, SN75452B, SN75453B, SN75454B
DUAL PERIPHERAL DRIVERS**

SLRS021B – DECEMBER 1976 – REVISED SEPTEMBER 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55'	SN75'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	V
Input voltage, V_I	5.5	5.5	V
Inter-emitter voltage (see Note 2)	5.5	5.5	V
Off-state output voltage, V_O	30	30	V
Continuous collector or output current, I_{OK} (see Note 3)	400	400	mA
Peak collector or output current, I_I ($t_W \leq 10$ ms, duty cycle $\leq 50\%$, see Note 4)	500	500	mA
Continuous total power dissipation	See Dissipation Rating Table		
Operating free-air temperature range, T_A	-55 to 125	0 to 70	°C
Storage temperature range, T_{stg}	-65 to 150	-65 to 150	°C
Case temperature for 60 seconds	FK package	260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260 °C

- NOTES: 1. Voltage values are with respect to network GND, unless otherwise specified.
 2. This is the voltage between two emitters of a multiple-emitter transistor.
 3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω .
 4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	—

recommended operating conditions

	SN55'			SN75'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}	0.8			0.8			V
Operating free-air temperature, T_A	-55 125			0 70			°C



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logic symbol†



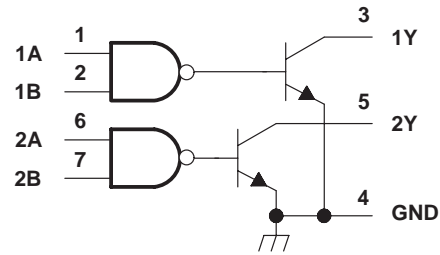
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.
Pin numbers shown are for the D, JG, and P packages.

FUNCTION TABLE
(each driver)

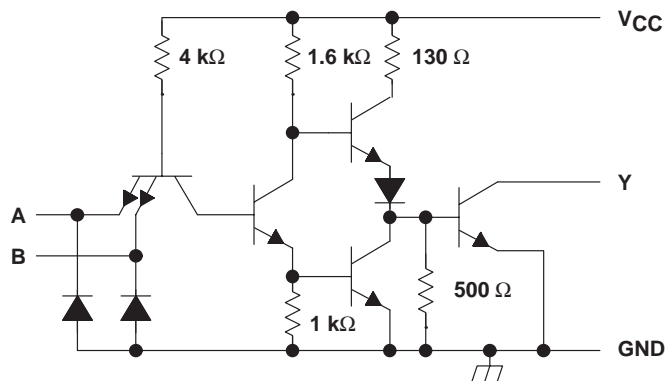
A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

positive logic:
 $Y = AB$ or $\overline{A+B}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS‡	SN55451B			SN75451B			UNIT
		MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$	-1.2	-1.5		-1.2	-1.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 100 \text{ mA}$	0.25	0.5		0.25	0.4		V
	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 300 \text{ mA}$	0.5	0.8		0.5	0.7		
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{OH} = 30 \text{ V}$			300			100	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$	-1	-1.6		-1	-1.6		mA
I_{CCH} Supply current, outputs high	$V_{CC} = \text{MAX}$, $V_I = 5 \text{ V}$	7	11		7	11		mA
I_{CCL} Supply current, outputs low	$V_{CC} = \text{MAX}$, $V_I = 0$	52	65		52	65		mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, See Figure 1		18	25	ns
t_{PHL} Propagation delay time, high-to-low-level output			18	25	
t_{TLH} Transition time, low-to-high-level output			5	8	
t_{THL} Transition time, high-to-low-level output			7	12	
V_{OH} High-level output voltage after switching	SN55451B	$V_S - 6.5$			mV
	SN75451B	$V_S - 6.5$			

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

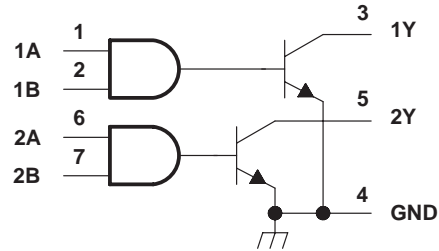
Pin numbers shown are for the D, JG, and P packages.

FUNCTION TABLE
(each driver)

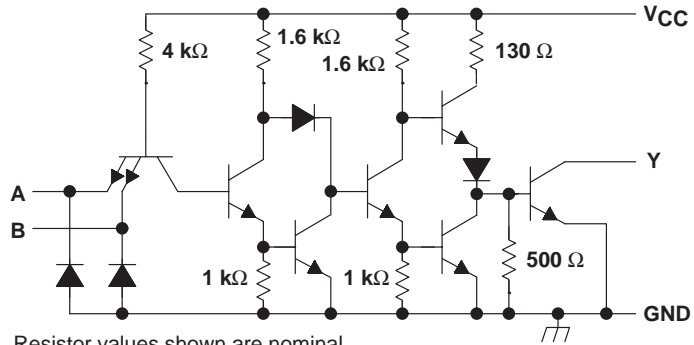
A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

positive logic:
 $Y = \overline{AB}$ or $\overline{A+B}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS‡	SN55452B			SN75452B			UNIT
		MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$	-1.2	-1.5		-1.2	-1.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $I_{OL} = 100 \text{ mA}$		0.25	0.5		0.25	0.4	V
	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $I_{OL} = 300 \text{ mA}$		0.5	0.8		0.5	0.7	
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $V_{OH} = 30 \text{ V}$			300			100	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.1			-1.1	mA
I_{CCH} Supply current, outputs high	$V_{CC} = \text{MAX}$, $V_I = 0$			11			11	mA
I_{CCL} Supply current, outputs low	$V_{CC} = \text{MAX}$, $V_I = 5 \text{ V}$			56			56	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

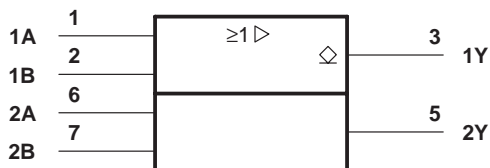
switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, See Figure 1		26	35	ns
t_{PHL} Propagation delay time, high-to-low-level output			24	35	
t_{TLH} Transition time, low-to-high-level output			5	8	
t_{THL} Transition time, high-to-low-level output			7	12	
V_{OH} High-level output voltage after switching	SN55452B	$V_S - 6.5$			mV
	SN75452B	$V_S - 6.5$			

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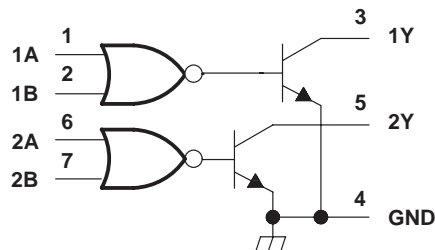
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logic symbol†

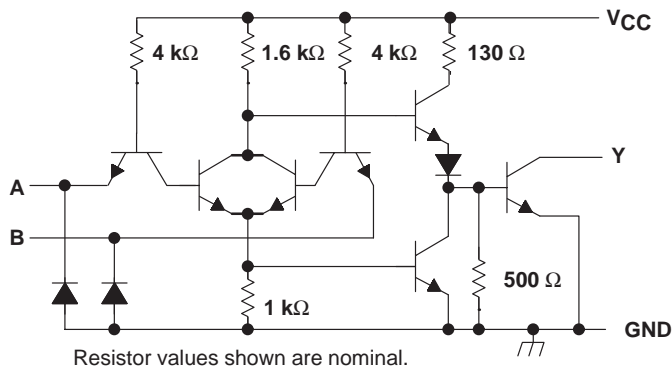


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12. Pin numbers shown are for the D, JG, and P packages.

logic diagram (positive logic)



schematic (each driver)



FUNCTION TABLE
(each driver)

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

positive logic:
 $Y = A+B$ or $\overline{A}\overline{B}$

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS‡	SN55453B		SN75453B		UNIT	
		MIN	TYP§	MAX	MIN		TYP§
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$	-1.2		-1.5	-1.2		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 100 \text{ mA}$	0.25		0.5	0.25		V
	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 300 \text{ mA}$	0.5		0.8	0.5		
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{OH} = 30 \text{ V}$			300		100	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1		1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40		40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$	-1		-1.6	-1	-1.6	mA
I_{CCH} Supply current, outputs high	$V_{CC} = \text{MAX}$, $V_I = 5 \text{ V}$	8		11	8	11	mA
I_{CCL} Supply current, outputs low	$V_{CC} = \text{MAX}$, $V_I = 0$	54		68	54	68	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

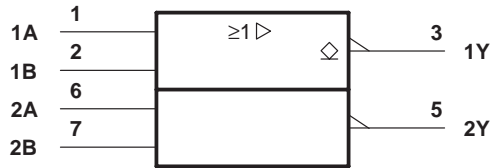
switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, See Figure 1		18	25	ns
t_{PHL} Propagation delay time, high-to-low-level output			18	25	
t_{TLH} Transition time, low-to-high-level output			5	8	
t_{THL} Transition time, high-to-low-level output			7	12	
V_{OH} High-level output voltage after switching	SN55453B	$V_S - 6.5$		mV	
	SN75453B	$V_S - 6.5$			

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logic symbol†



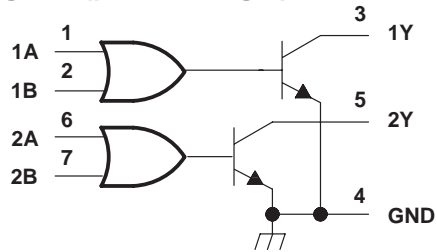
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FUNCTION TABLE
(each driver)

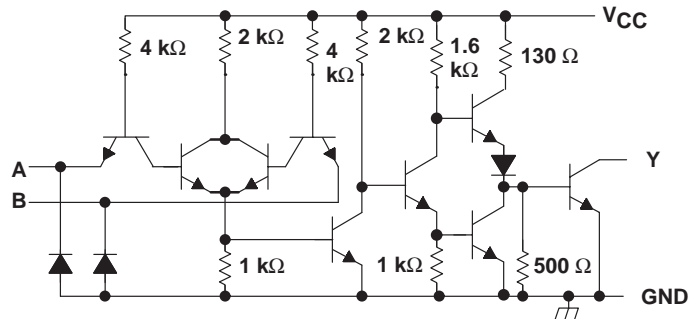
A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

positive logic:
 $Y = A+B$ or \overline{AB}

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS‡	SN55454B			SN75454B			UNIT
		MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$	-1.2	-1.5		-1.2	-1.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $I_{OL} = 100 \text{ mA}$	0.25	0.5		0.25	0.4		V
	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $I_{OL} = 300 \text{ mA}$	0.5	0.8		0.5	0.7		
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{OH} = 30 \text{ V}$, $V_{IL} = 0.8 \text{ V}$			300			100	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$	-1	-1.6		-1	-1.6		mA
I_{CCH} Supply current, outputs high	$V_{CC} = \text{MAX}$, $V_I = 0$	13	17		13	17		mA
I_{CCL} Supply current, outputs low	$V_{CC} = \text{MAX}$, $V_I = 5 \text{ V}$	61	79		61	79		mA

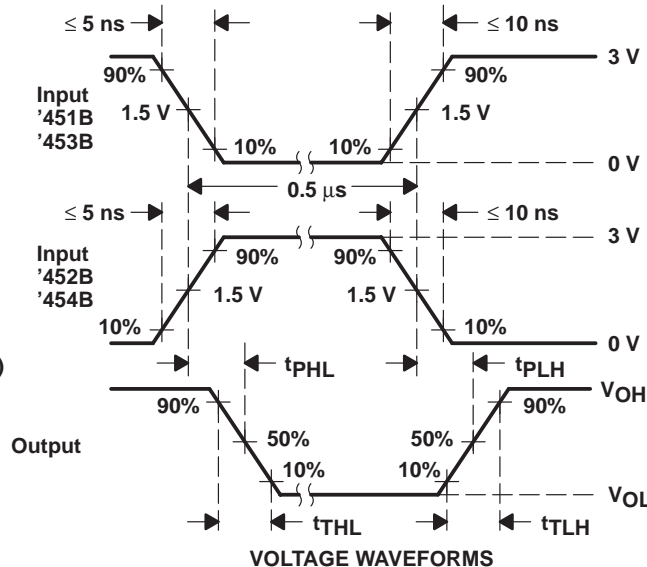
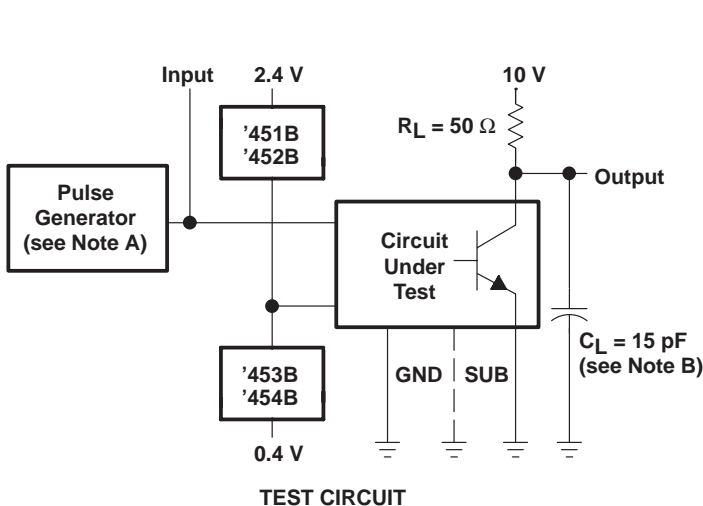
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

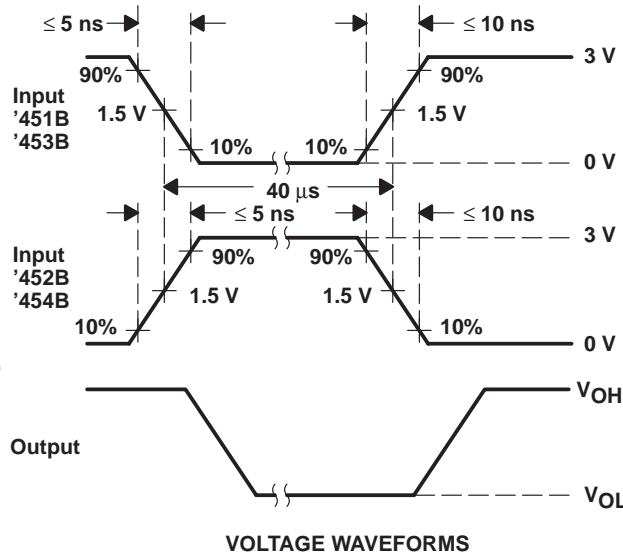
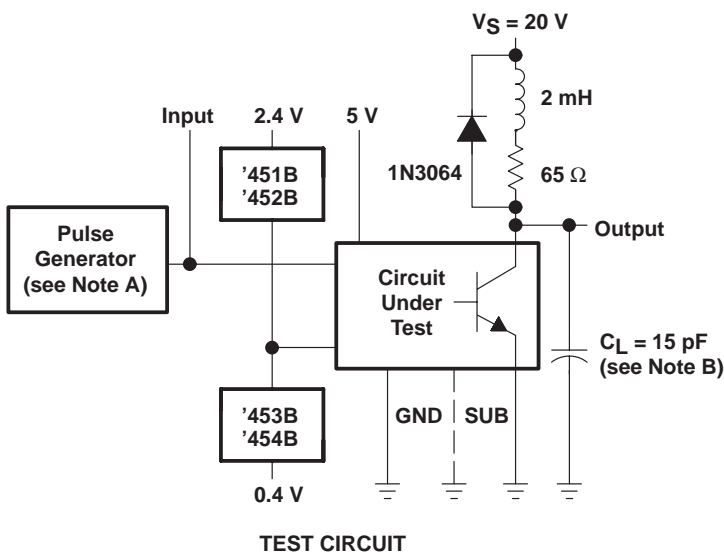
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH} Propagation delay time, low-to-high-level output	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, See Figure 1		27	35	ns	
t_{PHL} Propagation delay time, high-to-low-level output			24	35		
t_{TLH} Transition time, low-to-high-level output			5	8		
t_{THL} Transition time, high-to-low-level output			7	12		
V_{OH} High-level output voltage after switching	SN55454B	$V_S = 20 \text{ V}$, $I_O \approx 300 \text{ mA}$, See Figure 2			$V_S - 6.5$	mV
	SN75454B				$V_S - 6.5$	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Complete Drivers

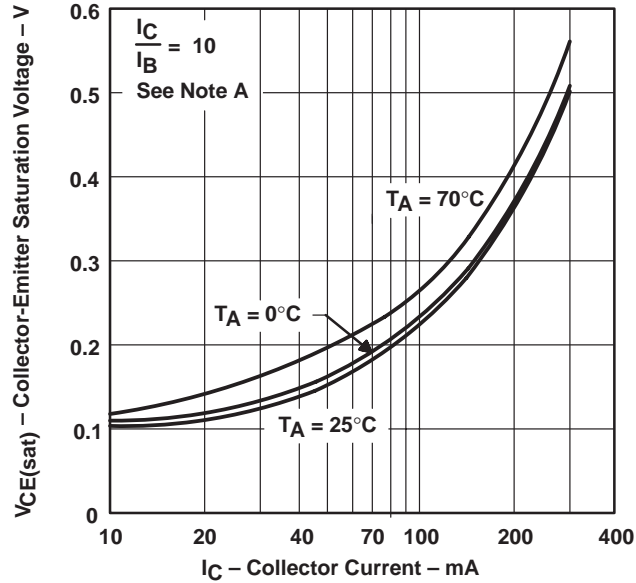


NOTES: A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms for Latch-Up Test of Complete Drivers

TYPICAL CHARACTERISTICS

TRANSISTOR
COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT



NOTE A: These parameters must be measured using pulse techniques, $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

Figure 3

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9563301Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
5962-9563301QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
77049012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
7704901PA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
77049022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
7704902PA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
JM38510/12902BPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
JM38510/12903BPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
JM38510/12905BPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
SN55451BJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
SN55452BJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
SN55453BJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
SN55454BJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
SN75451BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75451BDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75451BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75451BDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75451BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75451BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75451BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75451BPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75452BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75452BDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75452BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75452BDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75452BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75452BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75452BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75452BPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75453BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN75453BDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75453BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75453BDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75453BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75453BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75453BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75453BPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75454BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75454BDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75454BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75454BDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75454BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75454BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75454BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75454BPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ55451BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
SNJ55451BJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
SNJ55452BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
SNJ55452BJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
SNJ55453BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
SNJ55453BJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
SNJ55454BFK	OBSOLETE	LCCC	FK	20		TBD	POST-PLATE	Level-NC-NC-NC
SNJ55454BJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered

at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

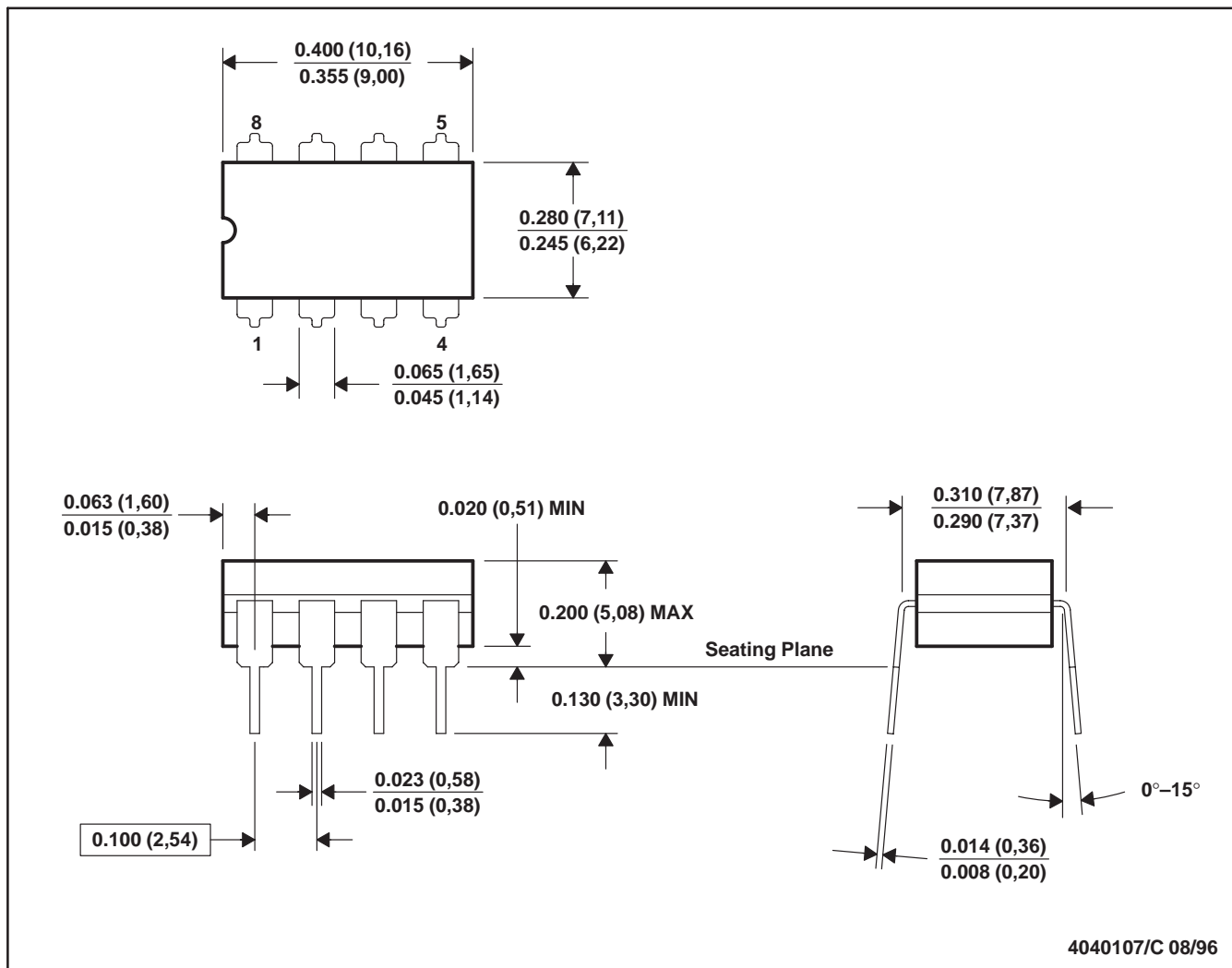
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE

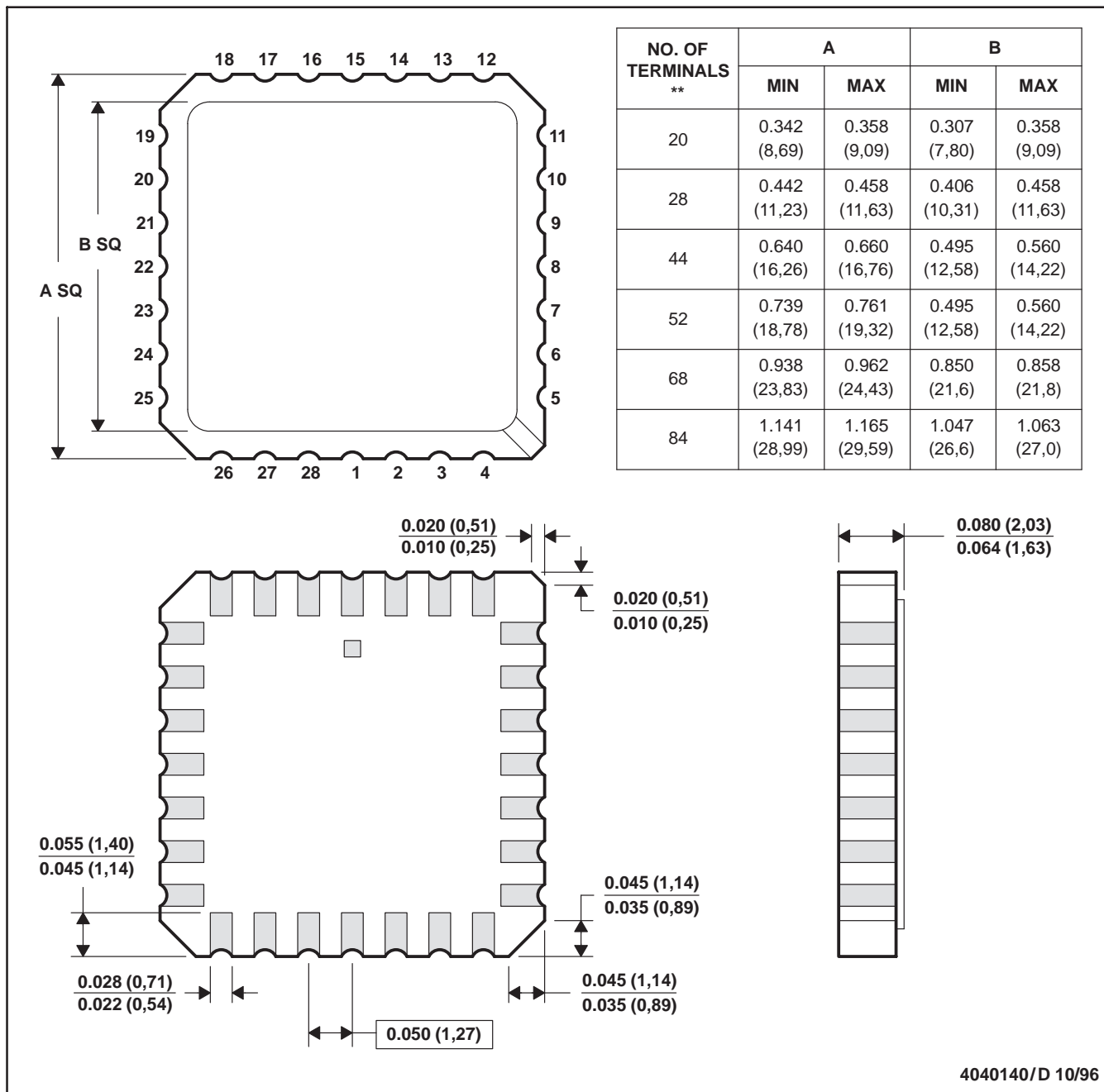


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

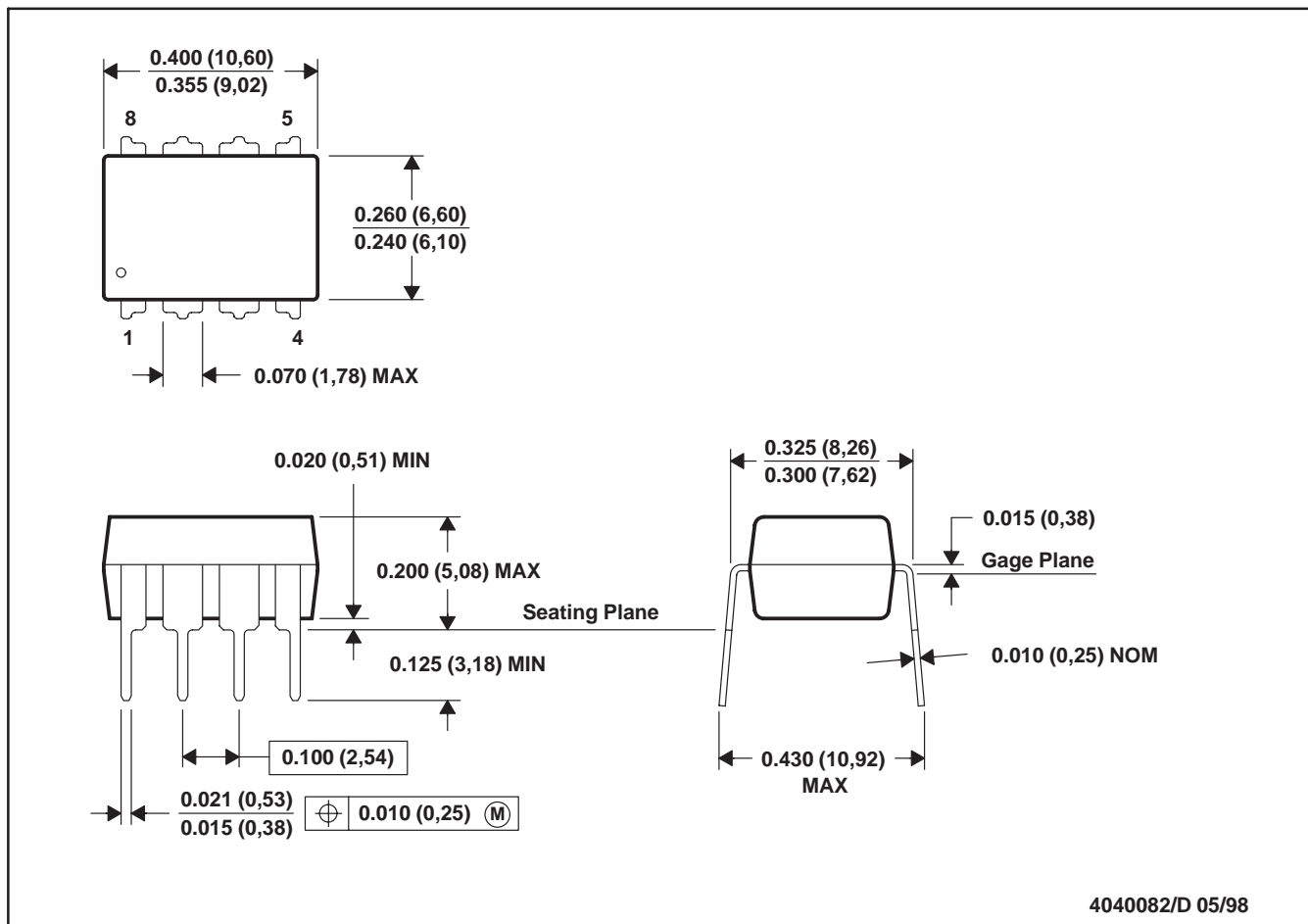
28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



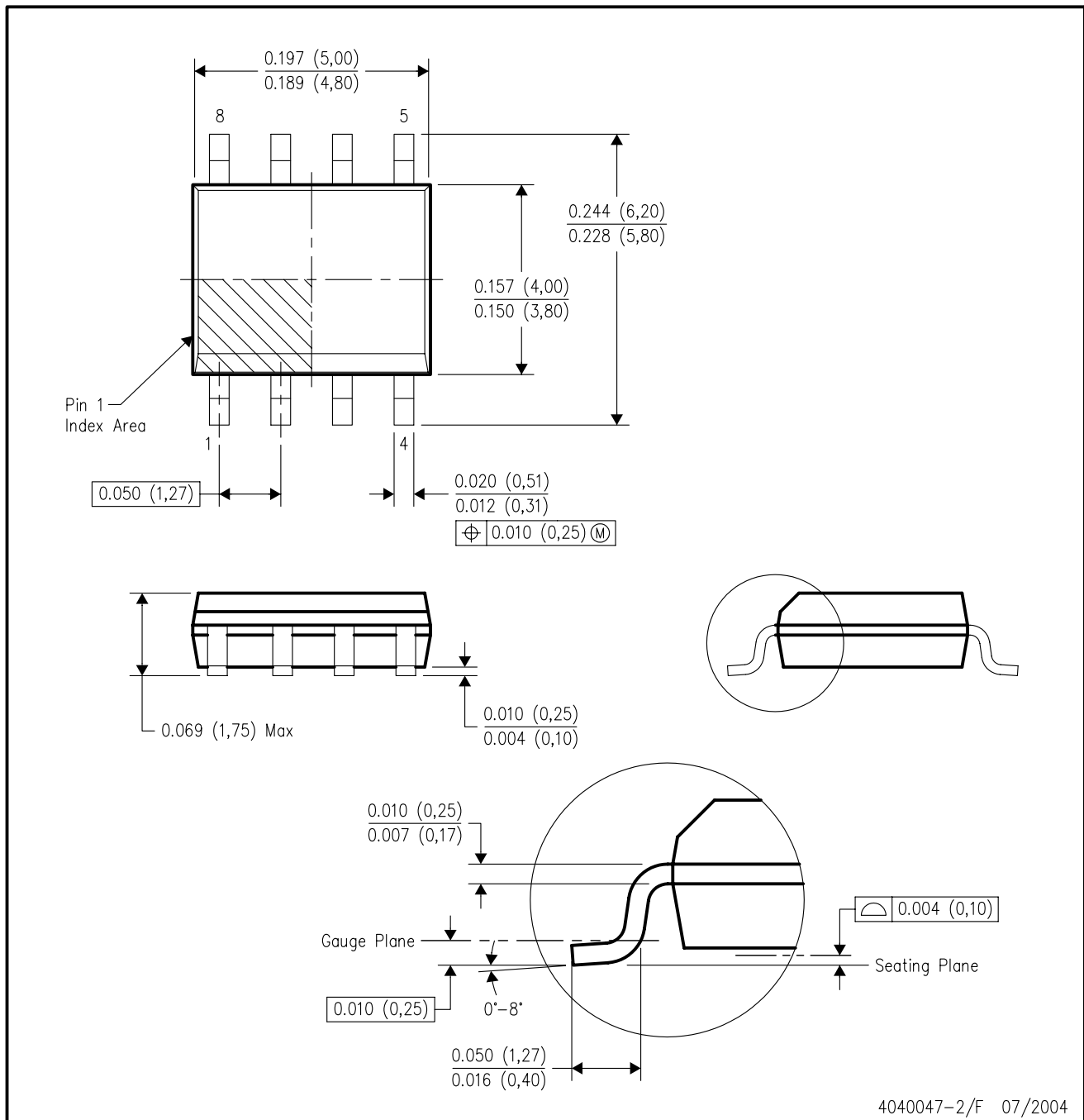
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm



D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

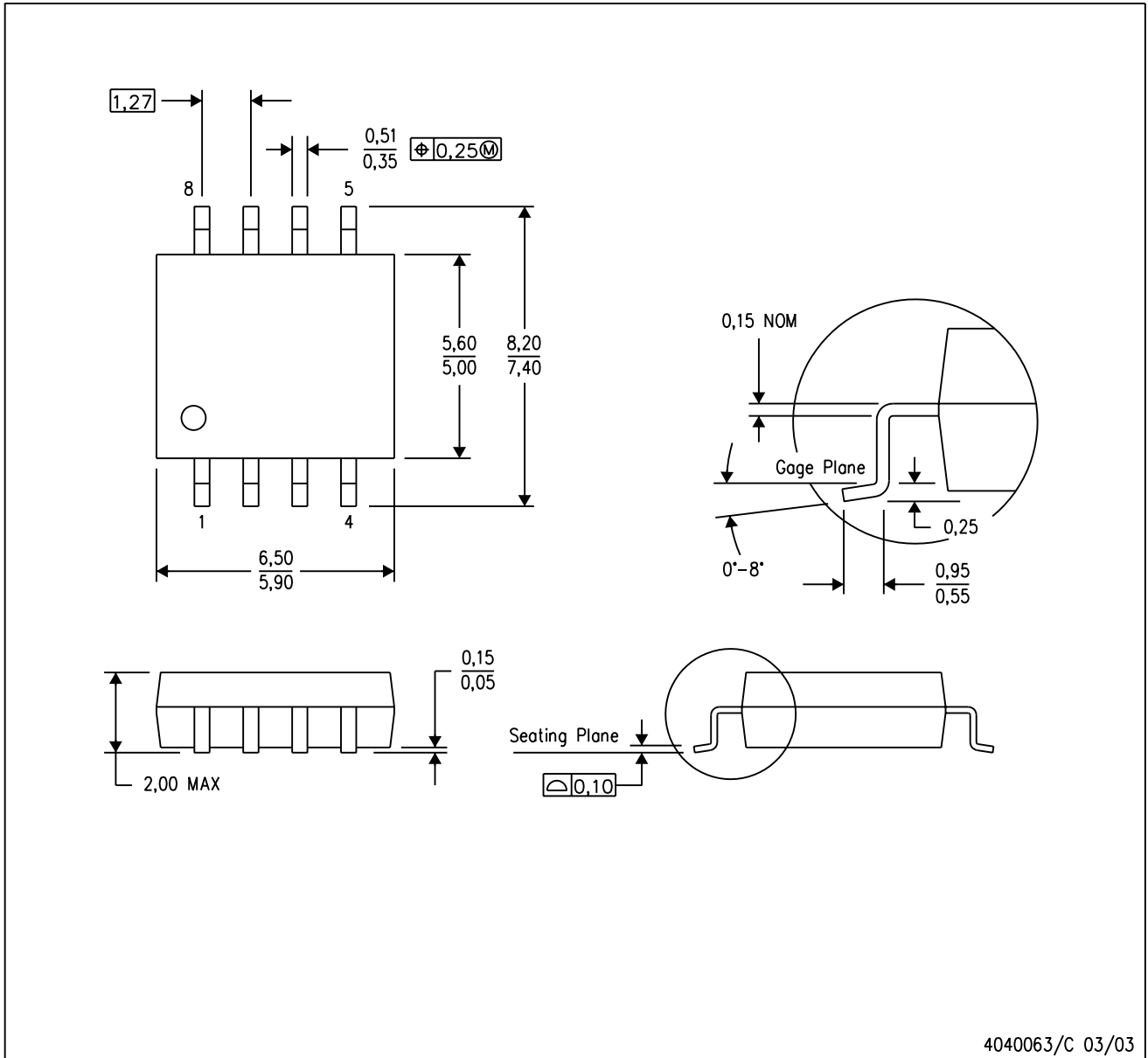


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AA.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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