- **Parallel Register Inputs ('LS592)**

- **Parallel 3-State I/O: Register Inputs/ Counter Outputs ('LS593)**

- **Counter has Direct Overriding Load and Clear**

- **Accurate Counter Frequency: DC to 20 MHz**

description

The 'LS592 comes in a 16-pin package and consists of a parallel input, 8-bit storage register feeding an 8-bit binary counter. Both the register and the counter have individual positive-edge-triggered clocks. In addition, the counter has direct load and clear functions. A low-going $\overline{RCO}$ pulse will be obtained when the counter reaches the hex word FF. Expansion is easily accomplished for two stages by connecting $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{RCO}$ of each stage to CCK of the following stage.

The 'LS593 comes in a 20-pin package and has all the features of the 'LS592 plus 3-state I/O, which provides parallel counter outputs. The tables below show the operation of the enable (CCKEN, $\overline{CCKEN}$) inputs. A register clock enable ($\overline{RCKEN}$) is also provided.

OUTPUT ENABLE CONTROL ('593 ONLY)

G	$\overline{G}$	A/QA thru H/QH
L	L	input mode
L	H	input mode
H	L	output mode
H	H	input mode

COUNTER CLOCK ENABLE CONTROL

CCKEN	$\overline{CCKEN}$	EFFECT ON CCK
L	L	Enable
L	H	Disable
H	L	Enable
H	H	Enable

SN54LS592 . . . J OR W PACKAGE
SN74LS592 . . . N PACKAGE
(TOP VIEW)

```
        B [1  U 16] VCC
        C [2     15] A
        D [3     14] CLOAD
        E [4     13] RCK
        F [5     12] CCKEN
        G [6     11] CCK
        H [7     10] CCLR
      GND [8      9] RCO
```
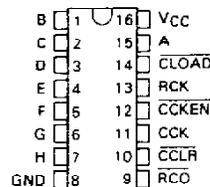
SN54LS592 . . . FK PACKAGE
(TOP VIEW)

```
              C  B  NC  VCC  A
             [3  2  1  20 19]
        D [4              18] CLOAD
        E [5              17] RCK
       NC [6              16] NC
        F [7              15] CCKEN
        G [8              14] CCK
             [9 10 11 12 13]
              H  GND NC RCO CCLR
```
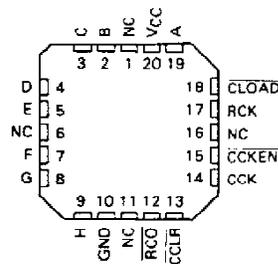
NC — No internal connection

SN54LS593 . . . J OR W PACKAGE
SN74LS593 . . . DW OR N PACKAGE
(TOP VIEW)

```
      A/QA [1  U 20] VCC
      B/QB [2     19] G
      C/QC [3     18] G̅
      D/QD [4     17] RCKEN
      E/QE [5     16] RCK
      F/QF [6     15] CCKEN
      G/QG [7     14] CCKEN
      H/QH [8     13] CCK
     CLOAD [9     12] CCLR
       GND [10    11] RCO
```
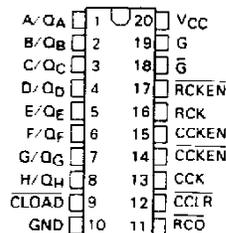
SN54LS593 . . . FK PACKAGE
(TOP VIEW)
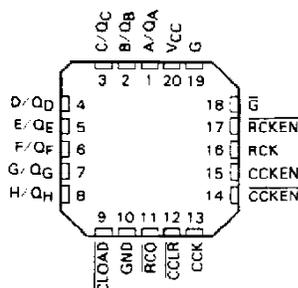
```
           C/QC B/QB A/QA VCC G
             [3  2  1  20 19]
     D/QD [4              18] G̅
     E/QE [5              17] RCKEN
     F/QF [6              16] RCK
     G/QG [7              15] CCKEN
     H/QH [8              14] CCKEN
             [9 10 11 12 13]
           CLOAD GND RCO CCLR CCK
```

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schematics of inputs and outputs

EQUIVALENT OF A THRU H INPUTS	EQUIVALENT OF 'LS592 CCK INPUT AND 'LS593 CCK AND RCK INPUTS	EQUIVALENT OF ALL OTHER INPUTS

'LS592 RCK: R_{eq} = 10 kΩ NOM
ALL OTHER: R_{eq} = 13 kΩ NOM

$\overline{RCO}$ OUTPUT	TYPICAL OF Q OUTPUTS ('LS593)

logic symbols†

'LS592

'LS593
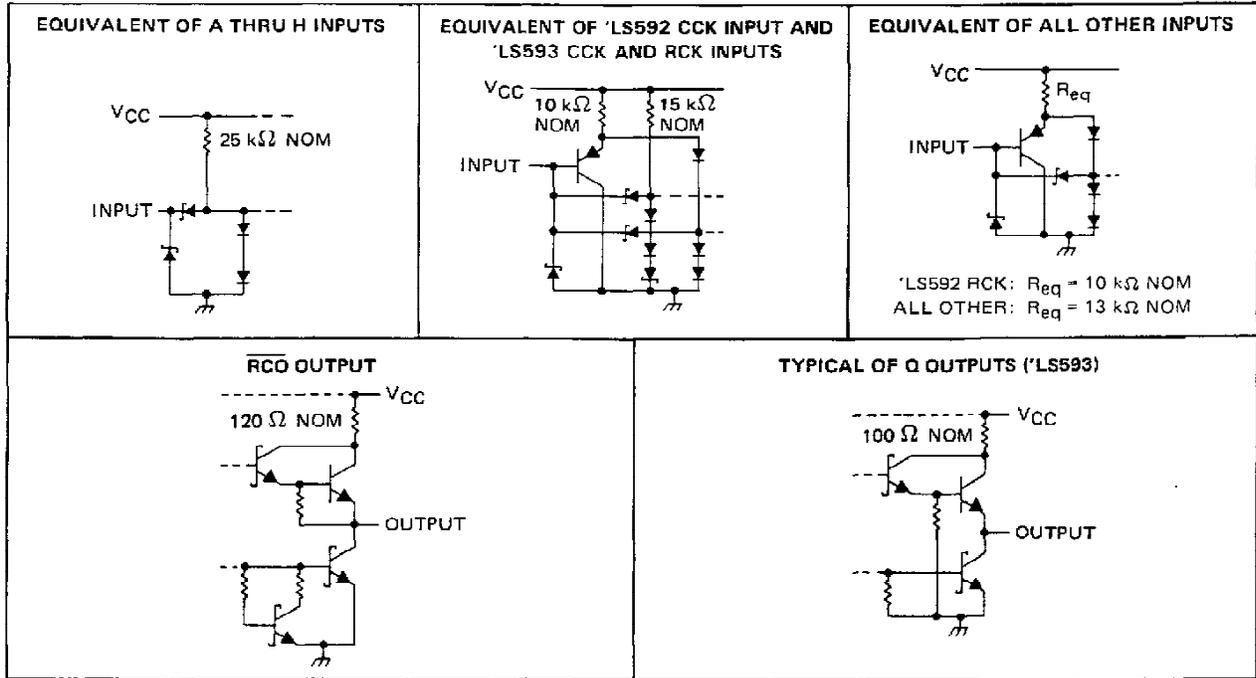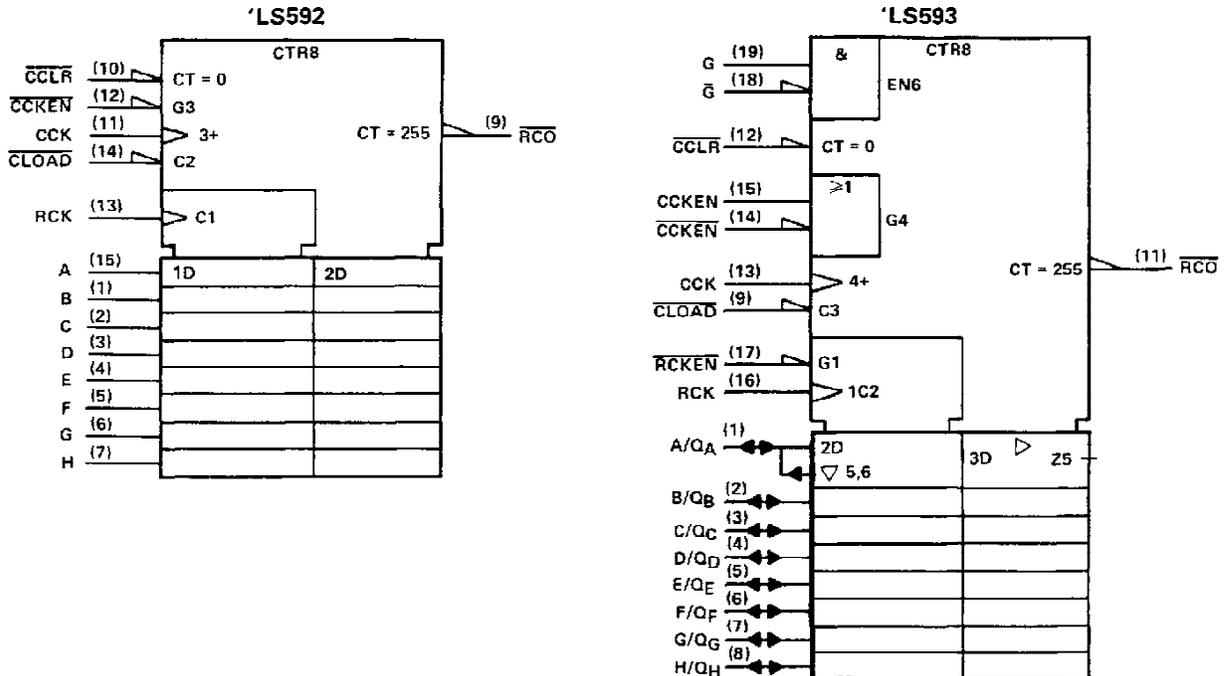

†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, N, and W packages.

logic diagram (positive logic)
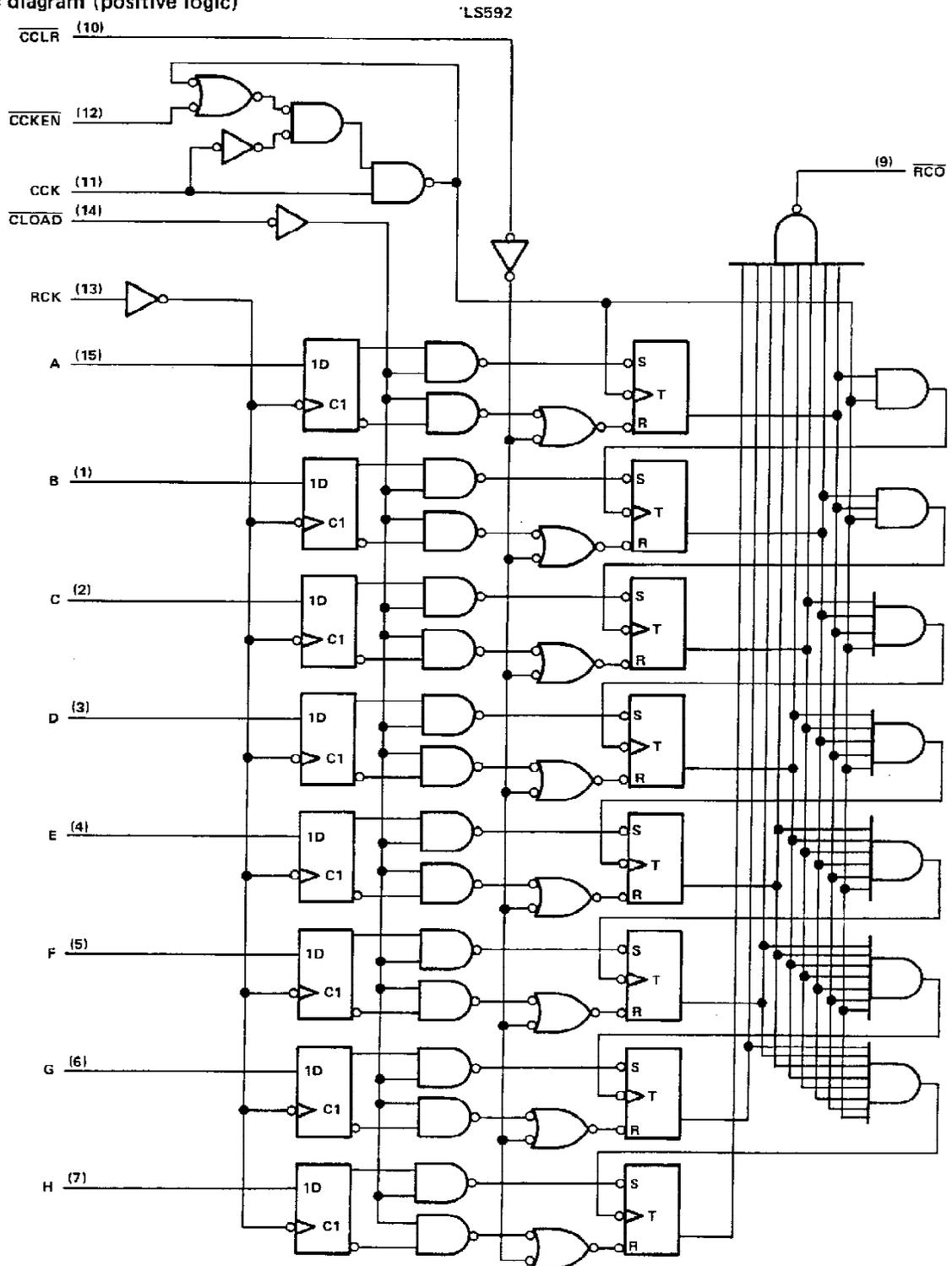
'LS592

Pin numbers shown are for J. N. and W packages.

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logic diagram (positive logic)

'LS593
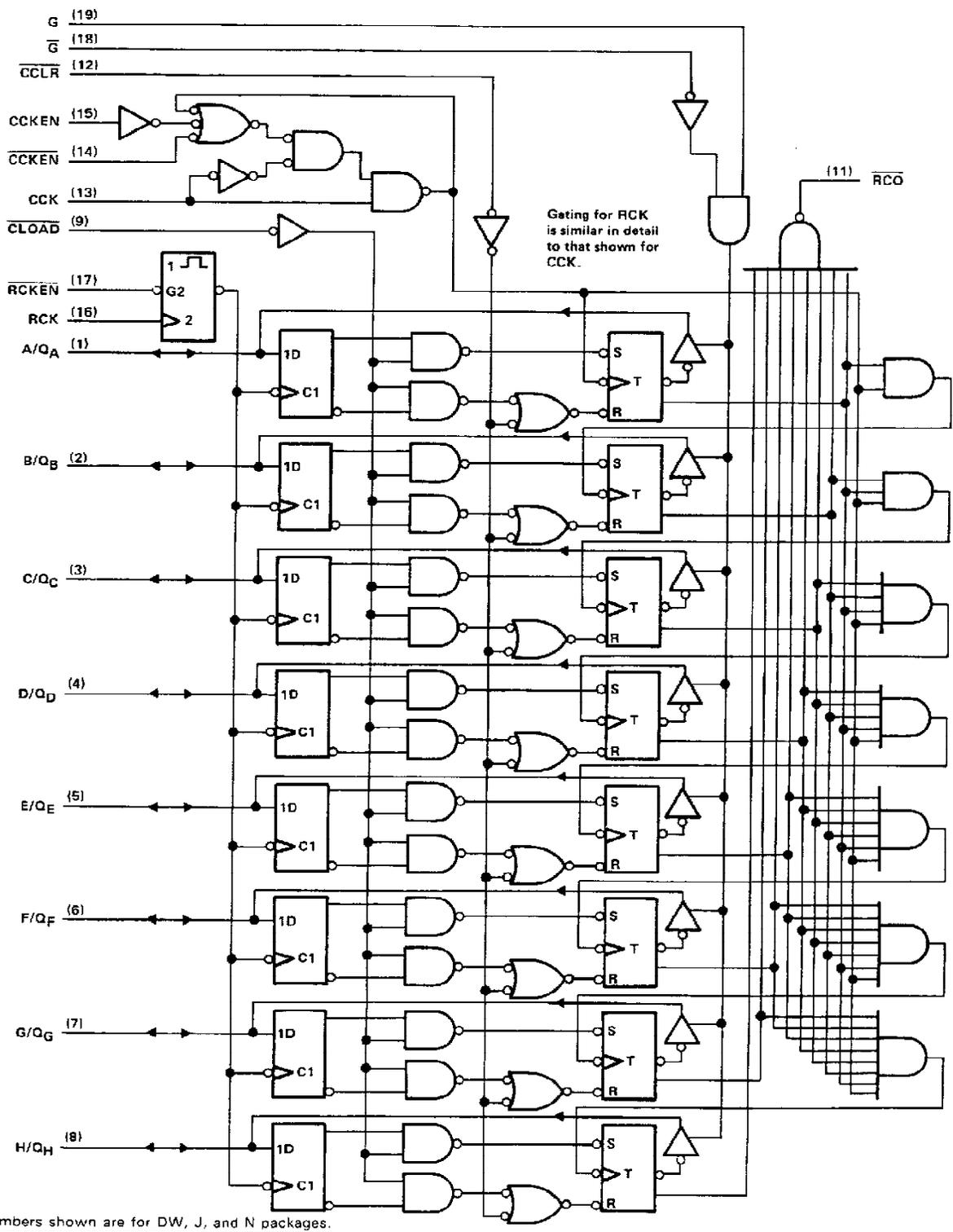
Gating for RCK
is similar in detail
to that shown for
CCK.

Pin numbers shown are for DW, J, and N packages.

typical operating sequences
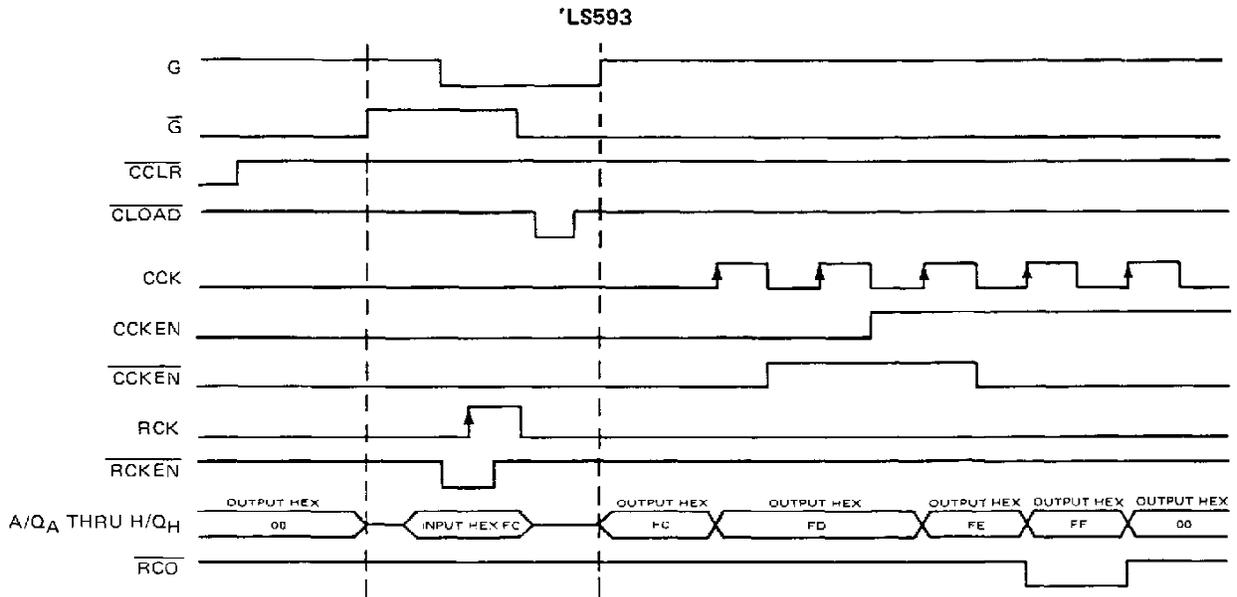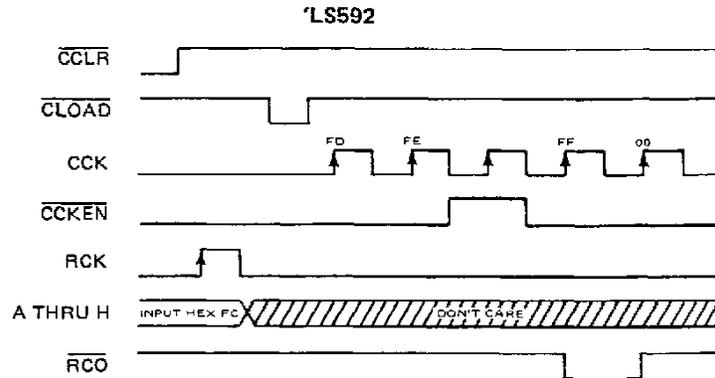
'LS592

'LS593

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage (excluding I/O ports) . . . . 7 V
Off-state output voltage (including I/O ports) . . . . 5.5 V
Operating free-air temperature range: SN54LS592, SN54LS593 . . . . −55°C to 125°C
SN74LS592, SN74LS593 . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current	$\overline{RCO}$			−1			−1	mA
		Q 'LS593 only			−1			−2.6	
I_{OL}	Low-level output current	$\overline{RCO}$			8			16	mA
		Q 'LS593 only			12			24	
f_{CCK}	Counter clock frequency		0		20	0		20	MHz
$t_{w\,(CCK)}$	Duration of counter clock pulse		25			25			ns
$t_{w\,(\overline{CCLR})}$	Duration of counter clear pulse		20			20			ns
$t_{w\,(RCK)}$	Duration of register clock pulse		20			20			ns
$t_{w\,(\overline{CLOAD})}$	Duration of counter load pulse		40			40			ns
t_{su}	Register enable setup time	$\overline{RCKEN}$ low to RCK ↑, 'LS593	20			20			ns
t_{su}	Counter enable setup time before CCK ↑	$\overline{CCKEN}$ low, 'LS592	30			30			ns
		$\overline{CCKEN}$ low or CCKEN high, 'LS593	30			30			
t_{su}	Setup time	$\overline{CCLR}$ inactive before CCK ↑	20			20			ns
		$\overline{CLOAD}$ inactive before CCK ↑	20			20			
		RCK ↑ before $\overline{CLOAD}$ ↑ (see Note 2)	30			30			
		Data A thru H before RCK ↑	20			20			
t_h	Hold time	Data A thru H after RCK ↑	0			0			ns
		All others	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 2: This time insures the data saved by RCK ↑ will also be loaded into the counter.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS' MIN	TYP‡	MAX	SN74LS' MIN	TYP‡	MAX	UNIT
V_{IK}			V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	'LS593 Q		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OH} = −1 mA	2.4	3.2					V
				I_{OH} = −2.6 mA				2.4	3.1		
	$\overline{RCO}$			I_{OH} = −1 mA	2.4	3.2		2.4	3.2		
V_{OL}	'LS593 Q		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
	$\overline{RCO}$			I_{OL} = 8 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 16 mA					0.35	0.5	
I_{OZH}	'LS593 Q		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = MAX, V_O = 2.7 V				20			20	µA
I_{OZL}	'LS593 Q		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = MAX, V_O = 0.4 V				−0.4			−0.4	mA
I_I	'LS593 Q		V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
	Others			V_I = 7 V			0.1			0.1	
I_{IH}			V_{CC} = MAX, V_I = 2.7 V				20			20	µA
I_{IL}	CCK		V_{CC} = MAX, V_I = 0.4 V				−0.8			−0.8	mA
	RCK	'LS592					−0.2			−0.2	
		'LS593					−0.8			−0.8	
	A thru H						−0.4			−0.4	
	Others						−0.2			−0.2	
I_{OS}§	'LS593 Q		V_{CC} = MAX, V_O = 0 V		−30		−130	−30		−130	mA
	$\overline{RCO}$				−20		−100	−20		−100	
I_{CC}	'LS592	I_{CCH}	V_{CC} = MAX, All possible inputs grounded, All outputs open			40	60		40	60	mA
		I_{CCL}				40	60		40	60	
	'LS593	I_{CCH}				47	70		47	70	
		I_{CCL}				53	80		53	80	
		I_{CCZ}				57	85		57	85	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

SN54LS592, SN54LS593, SN74LS592, SN74LS593
8-BIT BINARY COUNTERS WITH INPUT REGISTERS

switching characteristics, V_{CC} = 5 V, T_A = 25°C, (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		'LS592 MIN	'LS592 TYP	'LS592 MAX	'LS593 MIN	'LS593 TYP	'LS593 MAX	UNIT
f_{max}	CCK	$\overline{RCO}$	R_L = 1 kΩ,	C_L = 30 pF	20	35		20	35		MHz
t_{PLH}	CCK↑	Q							14	21	ns
t_{PHL}	CCK↑	Q							26	39	ns
t_{PLH}	$\overline{CLOAD}$↓	Q							34	51	ns
t_{PHL}	$\overline{CLOAD}$↓	Q							28	42	ns
t_{PHL}	$\overline{CCLR}$↓	Q	R_L = 667 Ω,	C_L = 45 pF					25	38	ns
t_{PZH}	G↑	Q							31	47	ns
t_{PZL}	G↑	Q							27	40	ns
t_{PZH}	$\overline{G}$↓	Q							29	45	ns
t_{PZL}	$\overline{G}$↓	Q							31	47	ns
t_{PHZ}	G↓	Q							33	50	ns
t_{PLZ}	G↓	Q	R_L = 667 Ω,	C_L = 5 pF					35	52	ns
t_{PHZ}	$\overline{G}$↑	Q							26	39	ns
t_{PLZ}	$\overline{G}$↑	Q							28	42	ns
t_{PLH}	CCK↑	$\overline{RCO}$			15		23	14		21	ns
t_{PHL}	CCK↑	$\overline{RCO}$			20		30	20		30	ns
t_{PLH}	$\overline{CLOAD}$↓	$\overline{RCO}$	R_L = 1 kΩ,	C_L = 30 pF	31		47	31		47	ns
t_{PHL}	$\overline{CLOAD}$↓	$\overline{RCO}$			27		41	27		41	ns
t_{PLH}	$\overline{CCLR}$↓	$\overline{RCO}$			30		45	30		45	ns
t_{PLH}	RCK↑	$\overline{RCO}$	R_L = 1 kΩ, C_L = 30 pF	$\overline{CLOAD}$ = L	35		53	42		63	ns
t_{PHL}	RCK↑	$\overline{RCO}$			30		45	33		50	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-87621012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
5962-8762101EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
5962-8762101EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
5962-8762101FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
5962-8762101FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SN54LS592J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN54LS592J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN54LS593J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN54LS593J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN74LS592D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LS592D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LS592DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LS592DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LS592DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LS592DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LS592DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LS592DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LS592N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS592N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS592N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS592N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS592NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS592NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS592NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS592NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74LS593DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS593N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS593N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS593N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS593NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS593NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS593NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS593NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54LS592FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS592FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS592J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS592J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS592W	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS592W	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS593FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS593FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS593J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS593J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS593W	OBSOLETE			20		TBD	Call TI	Call TI
SNJ54LS593W	OBSOLETE			20		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14) D

0.045 (1,14) D
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) M

14/18 Pin Only
20 Pin vendor option D

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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