

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4050B **buffers** **HEX non-inverting buffers**

Product specification
File under Integrated Circuits, IC04

January 1995

HEX non-inverting buffers

HEF4050B buffers

DESCRIPTION

The HEF4050B provides six non-inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. Their guaranteed fan-out into common bipolar logic elements is shown in the table below.

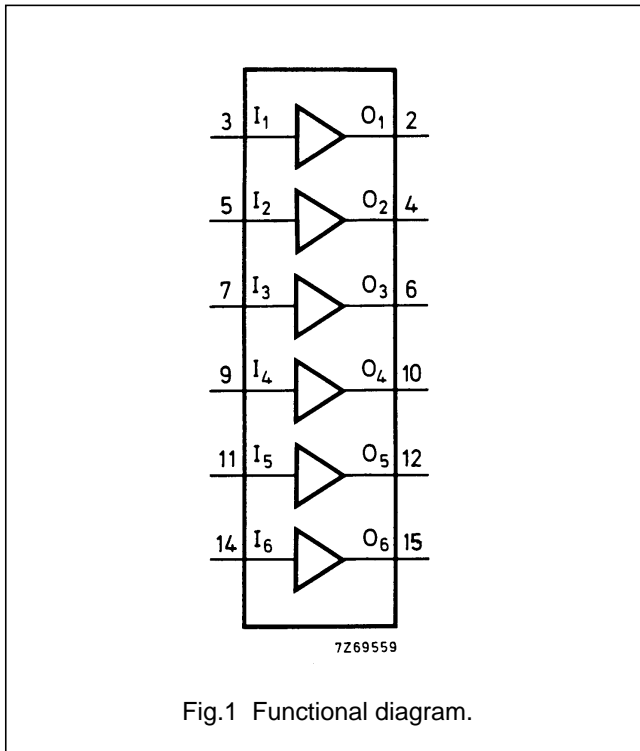


Fig.1 Functional diagram.

Guaranteed fan-out in common logic families

DRIVEN ELEMENT	GUARANTEED FAN-OUT
standard TTL	2
74 LS	9
74 L	16

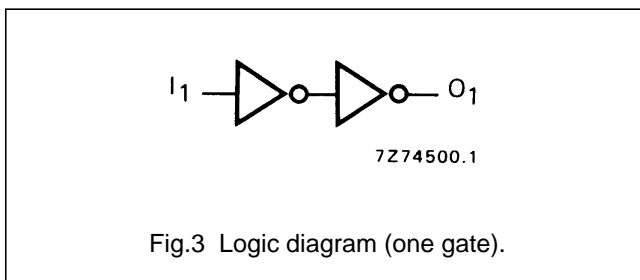


Fig.3 Logic diagram (one gate).

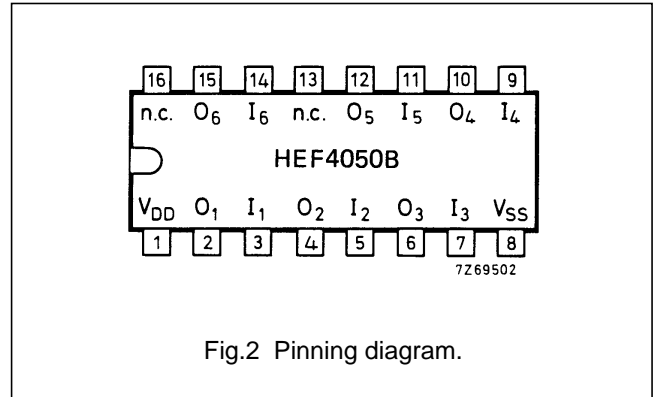


Fig.2 Pinning diagram.

- HEF4050BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4050BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4050BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

APPLICATION INFORMATION

Some examples of applications for the HEF4050B are:

- LOCMOS to DTL/TTL converter
- HIGH sink current for driving 2 TTL loads
- HIGH-to-LOW level logic conversion

Input protection

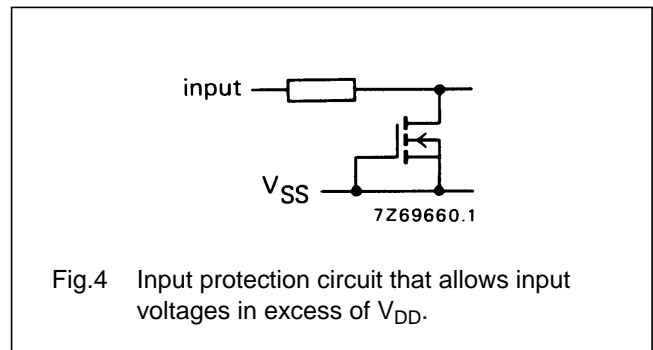


Fig.4 Input protection circuit that allows input voltages in excess of V_{DD} .

FAMILY DATA, I_{DD} LIMITS category BUFFERS

See Family Specifications

HEX non-inverting buffers

HEF4050B
buffers

DC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD}

HEF	V_{DD} V	V_O V	SYMBOL	T_{amb} (°C)						
				-40		+25		+85		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Output (sink) current LOW	4,75	0,4	I_{OL}	3,5	–	2,9	–	2,3	–	mA
	10	0,5		12,0	–	10,0	–	8,0	–	mA
	15	1,5		24,0	–	20,0	–	16,0	–	mA
Output (source) current HIGH	5	4,6	$-I_{OH}$	0,52	–	0,44	–	0,36	–	mA
	10	9,5		1,3	–	1,1	–	0,9	–	mA
	15	13,5		3,6	–	3,0	–	2,4	–	mA
Output (source) current HIGH	5	2,5	$-I_{OH}$	1,7	–	1,4	–	1,1	–	mA

HEC	V_{DD} V	V_O V	SYMBOL	T_{amb} (°C)						
				-55		+25		+125		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Output (sink) current LOW	4,75	0,4	I_{OL}	3,6	–	2,9	–	1,9	–	mA
	10	0,5		12,5	–	10,0	–	6,7	–	mA
	15	1,5		25,0	–	20,0	–	13,0	–	mA
Output (source) current HIGH	5	4,6	$-I_{OH}$	0,52	–	0,44	–	0,36	–	mA
	10	9,5		1,3	–	1,1	–	0,9	–	mA
	15	13,5		3,6	–	3,0	–	2,4	–	mA

HEX non-inverting buffers

HEF4050B
buffers**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays I_n O_n HIGH to LOW LOW to HIGH	5	t_{PHL}	35	70	ns	26 ns + (0,18 ns/pF) C_L
	10		20	35	ns	16 ns + (0,08 ns/pF) C_L
	15		15	30	ns	12 ns + (0,05 ns/pF) C_L
	5	t_{PLH}	55	110	ns	28 ns + (0,55 ns/pF) C_L
	10		25	55	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
Output transition times HIGH to LOW LOW to HIGH	5	t_{THL}	25	50	ns	7 ns + (0,35 ns/pF) C_L
	10		10	20	ns	3 ns + (0,14 ns/pF) C_L
	15		7	14	ns	2 ns + (0,09 ns/pF) C_L
	5	t_{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$3\,800 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$11\,600 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$65\,900 f_i + \sum (f_o C_L) \times V_{DD}^2$	