

## CMOS 2K x 8 TIMEKEEPER SRAM

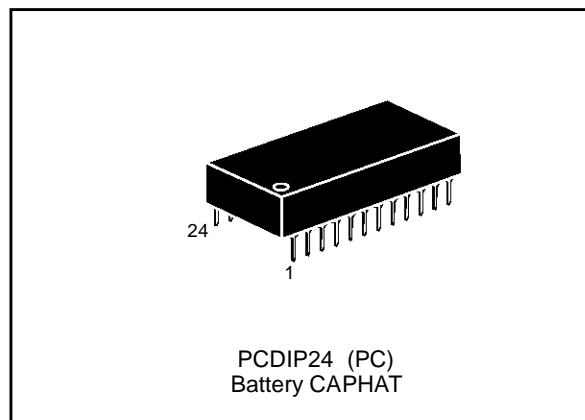
- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK and POWER-FAIL CONTROL CIRCUIT
- BYTEWISE RAM-LIKE CLOCK ACCESS
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES and SECONDS
- CLOCK ACCURACY of  $\pm 1$  MINUTE a MONTH, @ 25°C
- SOFTWARE CONTROLLED CLOCK CALIBRATION for HIGH ACCURACY APPLICATIONS
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48T02:  $4.5V \leq V_{PFD} \leq 4.75V$
  - M48T12:  $4.2V \leq V_{PFD} \leq 4.5V$
- SELF CONTAINED BATTERY and CRYSTAL in the CAPHAT DIP PACKAGE
- 10 YEARS of DATA RETENTION and CLOCK OPERATION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 2K x 8 SRAMs

### DESCRIPTION

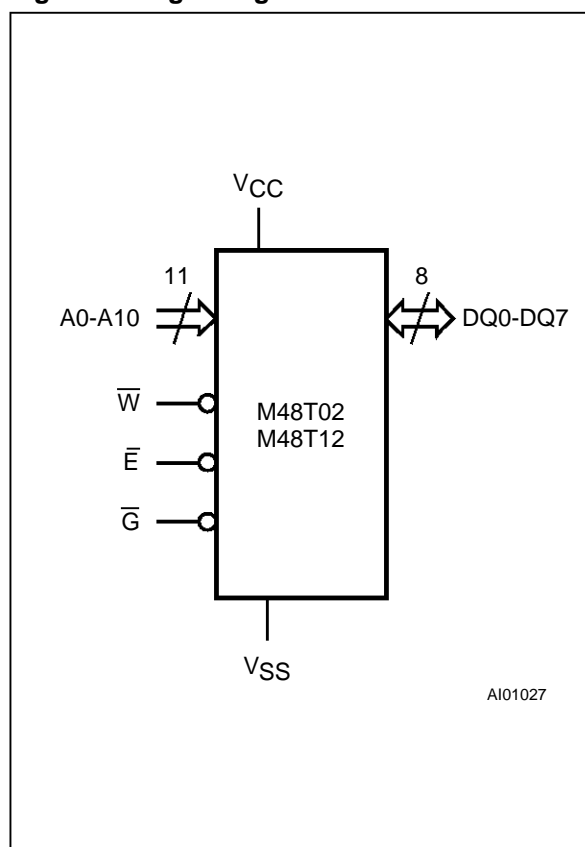
The M48T02,12 TIMEKEEPER™ RAM is a 2K x 8 non-volatile static RAM and real time clock which is pin and functional compatible with the MK48T02,12.

**Table 1. Signal Names**

A0-A10	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V <sub>CC</sub>	Supply Voltage
V <sub>SS</sub>	Ground



**Figure 1. Logic Diagram**



**Table 2. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
T <sub>A</sub>	Ambient Operating Temperature	0 to 70	°C
T <sub>STG</sub>	Storage Temperature (V <sub>CC</sub> Off, Oscillator Off)	–40 to 85	°C
V <sub>IO</sub>	Input or Output Voltages	–0.3 to 7	V
V <sub>CC</sub>	Supply Voltage	–0.3 to 7	V
I <sub>O</sub>	Output Current	20	mA
P <sub>D</sub>	Power Dissipation	1	W

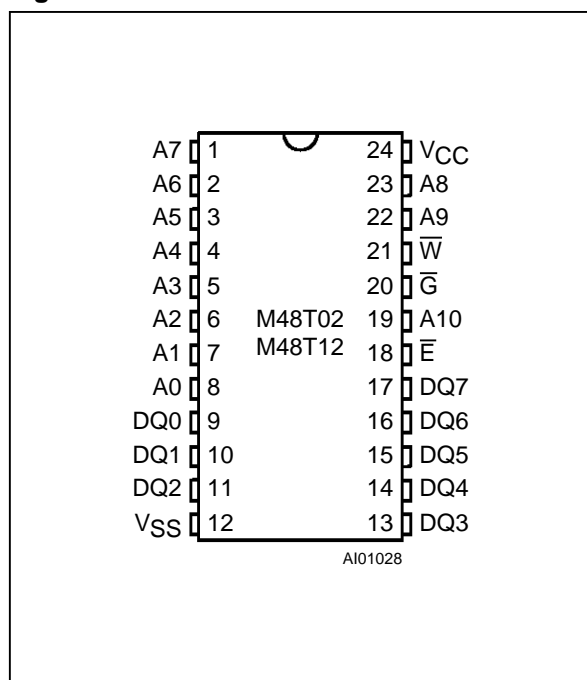
**Note:** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

**CAUTION:** Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.

**Table 3. Operating Modes**

Mode	V <sub>CC</sub>	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V <sub>IH</sub>	X	X	High Z	Standby
Write		V <sub>IL</sub>	X	V <sub>IL</sub>	D <sub>IN</sub>	Active
Read		V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>	Active
Read		V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	High Z	Active
Deselect	V <sub>SO</sub> to V <sub>PFD</sub> (min)	X	X	X	High Z	CMOS Standby
Deselect	≤ V <sub>SO</sub>	X	X	X	High Z	Battery Back-up Mode

**Note:** X = V<sub>IH</sub> or V<sub>IL</sub>

**Figure 2. DIP Pin Connections**

**DESCRIPTION (cont'd)**

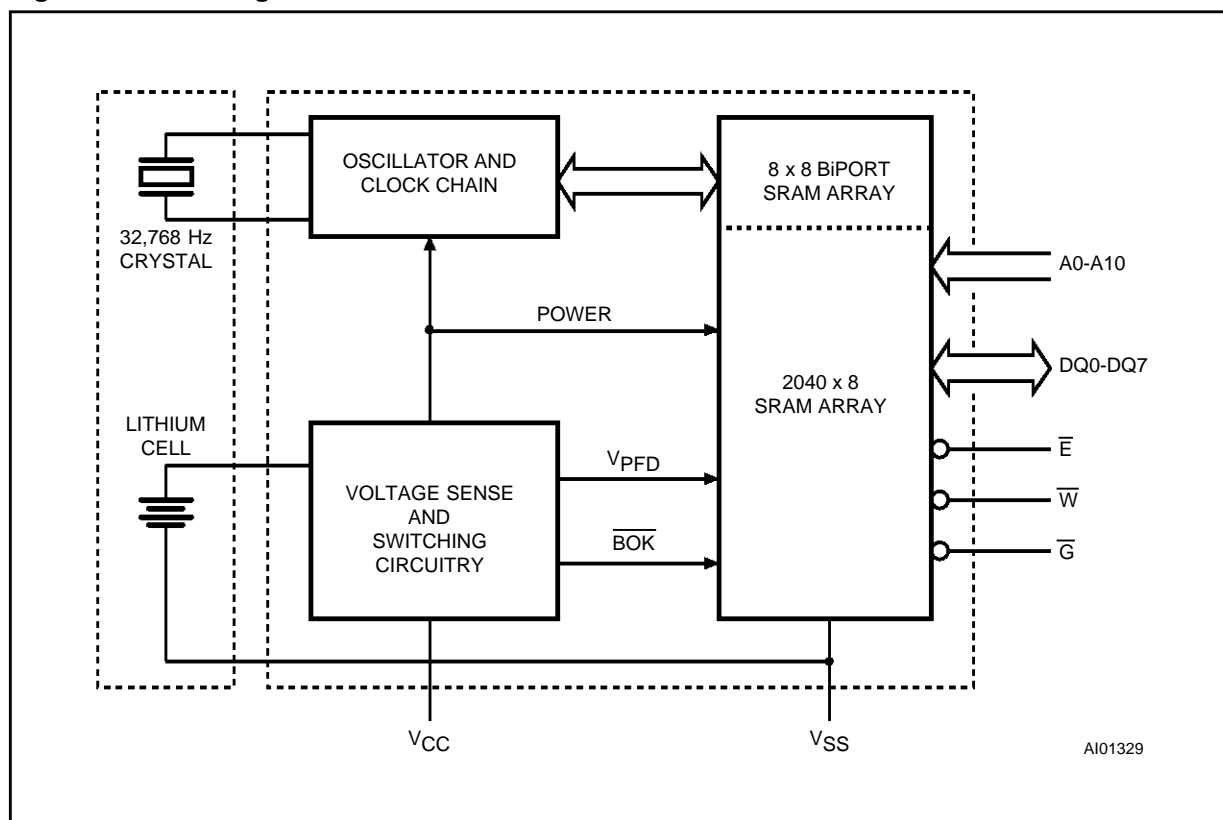
A special 24 pin 600mil DIP CAPHAT™ package houses the M48T02,12 silicon with a quartz crystal and a long life lithium button cell to form a highly integrated battery backed-up memory and real time clock solution.

The M48T02,12 button cell has sufficient capacity and storage life to maintain data and clock functionality for an accumulated time period of at least 10 years in the absence of power over the operating temperature range.

The M48T02,12 is a non-volatile pin and function equivalent to any JEDEC standard 2K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

As Figure 3 shows, the static memory array and the quartz controlled clock oscillator of the M48T02,12 are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE™

Figure 3. Block Diagram



clock information in the bytes with addresses 7F8h-7FFh. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. Byte 7F8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ read/write memory cells. The M48T02,12 includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

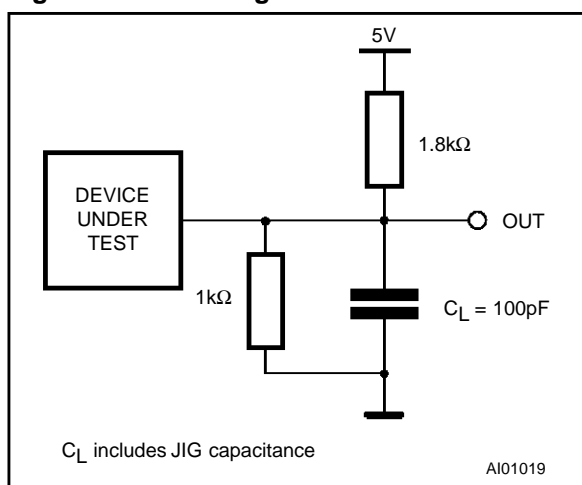
The M48T02,12 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When  $V_{CC}$  is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low  $V_{CC}$ . As  $V_{CC}$  falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

#### AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	$\leq 5\text{ns}$
Input Pulse Voltages	0.6V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit



**Table 4. Capacitance<sup>(1)</sup>** ( $T_A = 25\text{ }^{\circ}\text{C}$ ,  $f = 1\text{ MHz}$ )

Symbol	Parameter	Test Condition	Min	Max	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$		10	pF
$C_{IO}^{(2)}$	Input / Output Capacitance	$V_{OUT} = 0V$		10	pF

**Notes:** 1. Effective capacitance calculated from the equation  $C = I\Delta t/\Delta V$  with  $\Delta V = 3V$  and power supply at 5V.  
2. Outputs deselected

**Table 5. DC Characteristics** ( $T_A = 0\text{ to }70^{\circ}\text{C}$ ;  $V_{CC} = 4.75V\text{ to }5.5V\text{ or }4.5V\text{ to }5.5V$ )

Symbol	Parameter	Test Condition	Min	Max	Unit
$I_{LI}^{(1)}$	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		$\pm 1$	$\mu A$
$I_{LO}^{(1)}$	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		$\pm 5$	$\mu A$
$I_{CC}$	Supply Current	Outputs open		80	mA
$I_{CC1}^{(2)}$	Supply Current (Standby) TTL	$\bar{E} = V_{IH}$		3	mA
$I_{CC2}^{(2)}$	Supply Current (Standby) CMOS	$\bar{E} = V_{CC} - 0.2V$		3	mA
$V_{IL}^{(3)}$	Input Low Voltage		-0.3	0.8	V
$V_{IH}$	Input High Voltage		2.2	$V_{CC} + 0.3$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.1mA$		0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -1mA$	2.4		V

**Notes:** 1. Outputs Deselected.  
2. Measured with Control Bits set as follows: R = '1'; W, ST, KS, FT = '0'.  
3. Negative spikes of -1V allowed for up to 10ns once per Cycle.

**Table 6. Power Down/Up Trip Points DC Characteristics<sup>(1)</sup>** ( $T_A = 0\text{ to }70^{\circ}\text{C}$ )

Symbol	Parameter	Min	Typ	Max	Unit
$V_{PFD}$	Power-fail Deselect Voltage (M48T02)	4.5	4.6	4.75	V
$V_{PFD}$	Power-fail Deselect Voltage (M48T12)	4.2	4.3	4.5	V
$V_{SO}$	Battery Back-up Switchover Voltage		3.0		V
$t_{DR}^{(2)}$	Expected Data Retention Time	10			YEARS

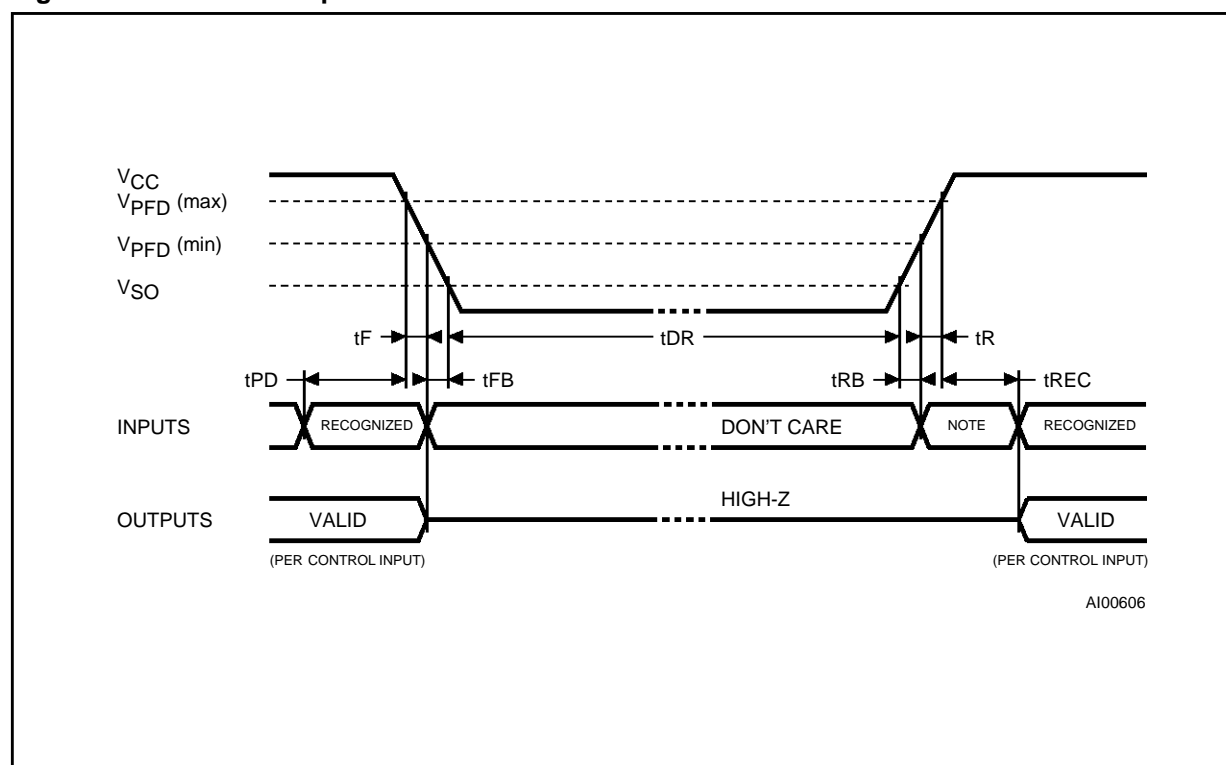
**Notes:** 1. All voltages referenced to  $V_{SS}$ .  
2. @  $25^{\circ}\text{C}$

**Table 7. Power Down/Up Mode AC Characteristics** ( $T_A = 0$  to  $70^\circ\text{C}$ )

Symbol	Parameter	Min	Max	Unit
$t_{PD}$	$\overline{E}$ or $\overline{W}$ at $V_{IH}$ before Power Down	0		$\mu\text{s}$
$t_F^{(1)}$	$V_{PFD}(\text{max})$ to $V_{PFD}(\text{min})$ $V_{CC}$ Fall Time	300		$\mu\text{s}$
$t_{FB}^{(2)}$	$V_{PFD}(\text{min})$ to $V_{SO}$ $V_{CC}$ Fall Time	10		$\mu\text{s}$
$t_R$	$V_{PFD}(\text{min})$ to $V_{PFD}(\text{max})$ $V_{CC}$ Rise Time	0		$\mu\text{s}$
$t_{RB}$	$V_{SO}$ to $V_{PFD}(\text{min})$ $V_{CC}$ Rise Time	1		$\mu\text{s}$
$t_{REC}$	$\overline{E}$ or $\overline{W}$ at $V_{IH}$ after Power Up	2		ms

**Notes:** 1.  $V_{PFD}(\text{max})$  to  $V_{PFD}(\text{min})$  fall time of less than  $t_F$  may result in deselection/write protection not occurring until  $50 \mu\text{s}$  after  $V_{CC}$  passes  $V_{PFD}(\text{min})$ .

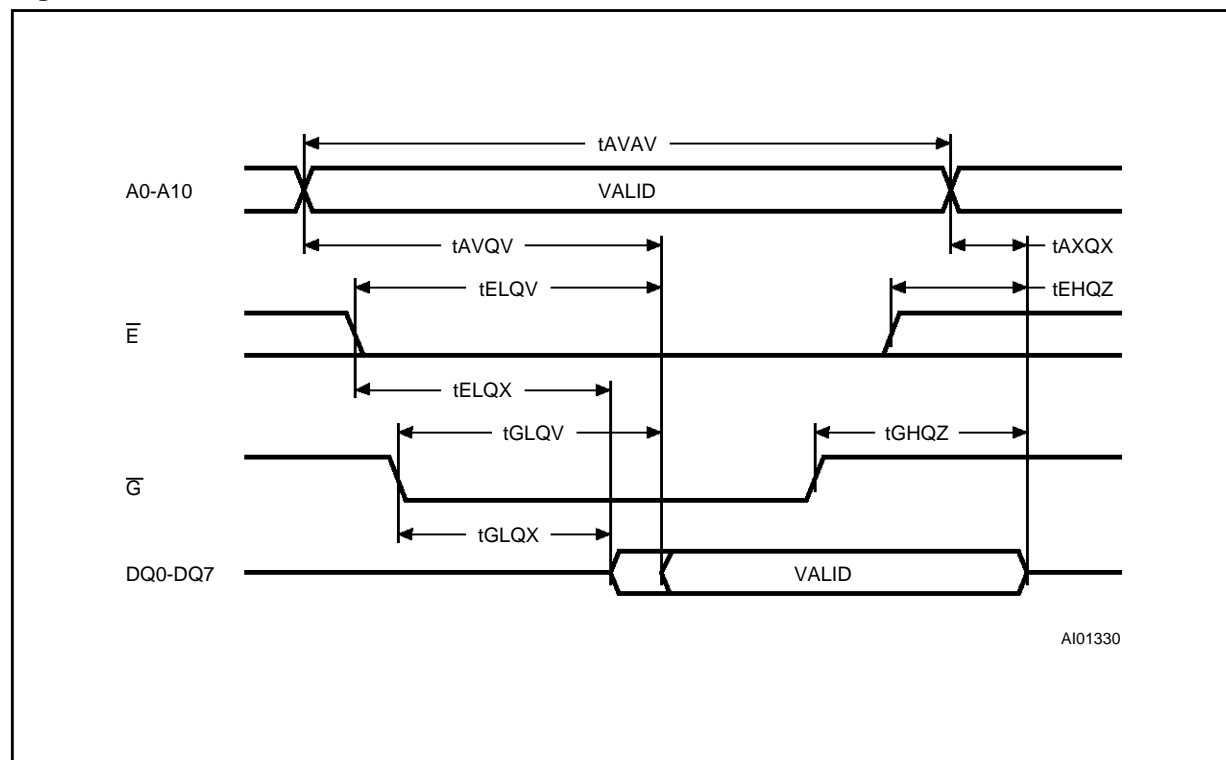
2.  $V_{PFD}(\text{min})$  to  $V_{SO}$  fall time of less than  $t_{FB}$  may cause corruption of RAM data.

**Figure 5. Power Down/Up Mode AC Waveforms**

**Note:** Inputs may or may not be recognized at this time. Caution should be taken to keep  $\overline{E}$  high as  $V_{CC}$  rises past  $V_{PFD}(\text{min})$ . Some systems may perform inadvertent write cycles after  $V_{CC}$  rises above  $V_{PFD}(\text{min})$  but before normal system operations begin. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

**Table 8. Read Mode AC Characteristics** ( $T_A = 0$  to  $70^\circ\text{C}$ ;  $V_{CC} = 4.75\text{V}$  to  $5.5\text{V}$  or  $4.5\text{V}$  to  $5.5\text{V}$ )

Symbol	Parameter	M48T02 / 12						Unit
		-120		-150		-200		
		Min	Max	Min	Max	Min	Max	
t <sub>AVAV</sub>	Read Cycle Time	120		150		200		ns
t <sub>AVQV</sub>	Address Valid to Output Valid		120		150		200	ns
t <sub>ELQV</sub>	Chip Enable Low to Output Valid		120		150		200	ns
t <sub>GLQV</sub>	Output Enable Low to Output Valid		75		75		80	ns
t <sub>ELQX</sub>	Chip Enable Low to Output Transition	10		10		10		ns
t <sub>GLQX</sub>	Output Enable Low to Output Transition	5		5		5		ns
t <sub>EHQZ</sub>	Chip Enable High to Output Hi-Z		30		35		40	ns
t <sub>GHQZ</sub>	Output Enable High to Output Hi-Z		30		35		40	ns
t <sub>AXQX</sub>	Address Transition to Output Transition	5		5		5		ns

**Figure 6. Read Mode AC Waveforms**

**Table 9. Write Mode AC Characteristics** ( $T_A = 0$  to  $70^\circ\text{C}$ ;  $V_{CC} = 4.75\text{V}$  to  $5.5\text{V}$  or  $4.5\text{V}$  to  $5.5\text{V}$ )

Symbol	Parameter	M48T02 / 12						Unit
		-120		-150		-200		
		Min	Max	Min	Max	Min	Max	
t <sub>AVAV</sub>	Write Cycle Time	120		150		200		ns
t <sub>AVWL</sub>	Address Valid to Write Enable Low	0		0		0		ns
t <sub>AVEL</sub>	Address Valid to Chip Enable Low	0		0		0		ns
t <sub>WLWH</sub>	Write Enable Pulse Width	75		90		120		ns
t <sub>ELEH</sub>	Chip Enable Low to Chip Enable High	75		90		120		ns
t <sub>WHAX</sub>	Write Enable High to Address Transition	10		10		10		ns
t <sub>EHAX</sub>	Chip Enable High to Address Transition	10		10		10		ns
t <sub>DVWH</sub>	Input Valid to Write Enable High	35		40		60		ns
t <sub>DVEH</sub>	Input Valid to Chip Enable High	35		40		60		ns
t <sub>WHDX</sub>	Write Enable High to Input Transition	5		5		5		ns
t <sub>EHDX</sub>	Chip Enable High to Input Transition	5		5		5		ns
t <sub>WLQZ</sub>	Write Enable Low to Output Hi-Z		40		50		60	ns
t <sub>AVWH</sub>	Address Valid to Write Enable High	90		120		140		ns
t <sub>AVEH</sub>	Address Valid to Chip Enable High	90		120		140		ns
t <sub>WHQX</sub>	Write Enable High to Output Transition	10		10		10		ns

## READ MODE

The M48T02,12 is in the Read Mode whenever  $\overline{W}$  (Write Enable) is high and  $\overline{E}$  (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs defines which one of the 2,048 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within  $t_{AVQV}$  (Address Access Time) after the last address input signal is stable, providing that the  $\overline{E}$  and  $\overline{G}$  access times are also satisfied. If the  $\overline{E}$  and  $\overline{G}$  access times are not met, valid data will be available after the latter of the Chip Enable Access Time ( $t_{ELQV}$ ) or Output Enable Access Time ( $t_{GLQV}$ ).

The state of the eight three-state Data I/O signals is controlled by  $\overline{E}$  and  $\overline{G}$ . If the outputs are activated before  $t_{AVQV}$ , the data lines will be driven to an indeterminate state until  $t_{VQV}$ . If the Address Inputs are changed while  $\overline{E}$  and  $\overline{G}$  remain active, output

data will remain valid for  $t_{AXQX}$  (Output Data Hold Time) but will go indeterminate until the next Address Access.

## WRITE MODE

The M48T02,12 is in the Write Mode whenever  $\overline{W}$  and  $\overline{E}$  are active. The start of a write is referenced from the latter occurring falling edge of  $\overline{W}$  or  $\overline{E}$ . A write is terminated by the earlier rising edge of  $\overline{W}$  or  $\overline{E}$ . The addresses must be held valid throughout the cycle.  $\overline{E}$  or  $\overline{W}$  must return high for minimum of  $t_{EHAX}$  from Chip Enable or  $t_{WHAX}$  from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid  $t_{DVWH}$  prior to the end of write and remain valid for  $t_{WHDX}$  afterward.  $\overline{G}$  should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on  $\overline{E}$  and  $\overline{G}$ , a low on  $\overline{W}$  will disable the outputs  $t_{WLQZ}$  after  $\overline{W}$  falls.

Figure 7. Write Enable Controlled, Write AC Waveforms

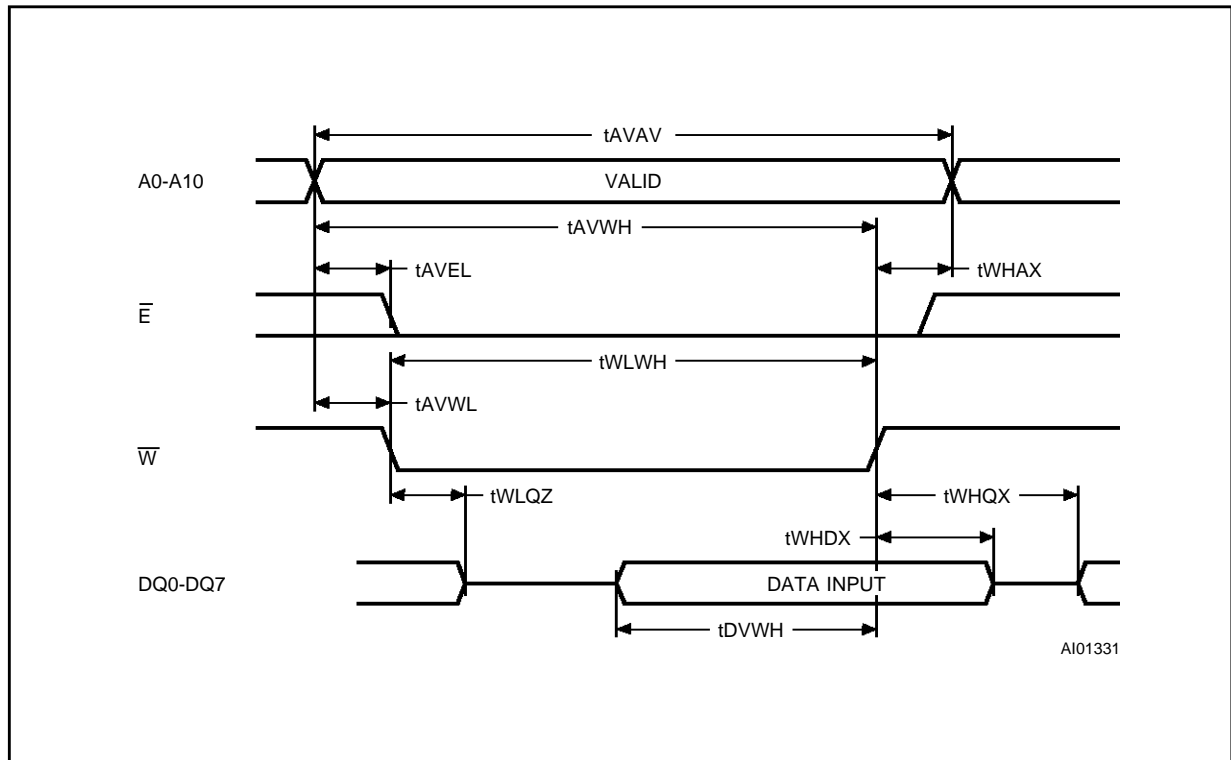
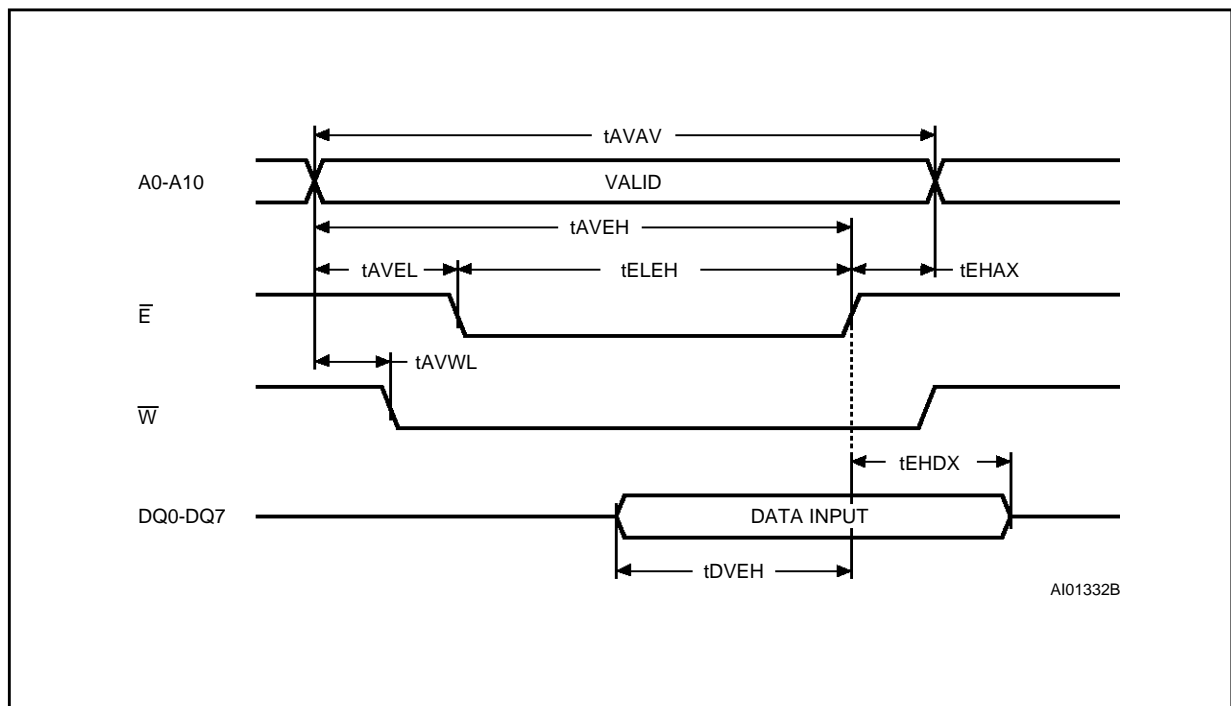


Figure 8. Chip Enable Controlled, Write AC Waveforms





## DATA RETENTION MODE

With valid  $V_{CC}$  applied, the M48T02,12 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when  $V_{CC}$  falls within the  $V_{PFD(max)}$ ,  $V_{PFD(min)}$  window. All outputs become high impedance, and all inputs are treated as "don't care."

**Note:** A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below  $V_{PFD(min)}$ , the user can be assured the memory will be in a write protected state, provided the  $V_{CC}$  fall time is not less than  $t_F$ . The M48T02,12 may respond to transient noise spikes on  $V_{CC}$  that reach into the deselect window during the time the device is sampling  $V_{CC}$ . Therefore, decoupling of the power supply lines is recommended.

The power switching circuit connects external  $V_{CC}$  to the RAM and disconnects the battery when  $V_{CC}$  rises above  $V_{SO}$ . As  $V_{CC}$  rises, the battery voltage is checked. If the voltage is too low, an internal Battery Not OK (BOK) flag will be set. The BOK flag can be checked after power up. If the BOK flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 9 illustrates how a BOK check routine could be structured.

## CLOCK OPERATIONS

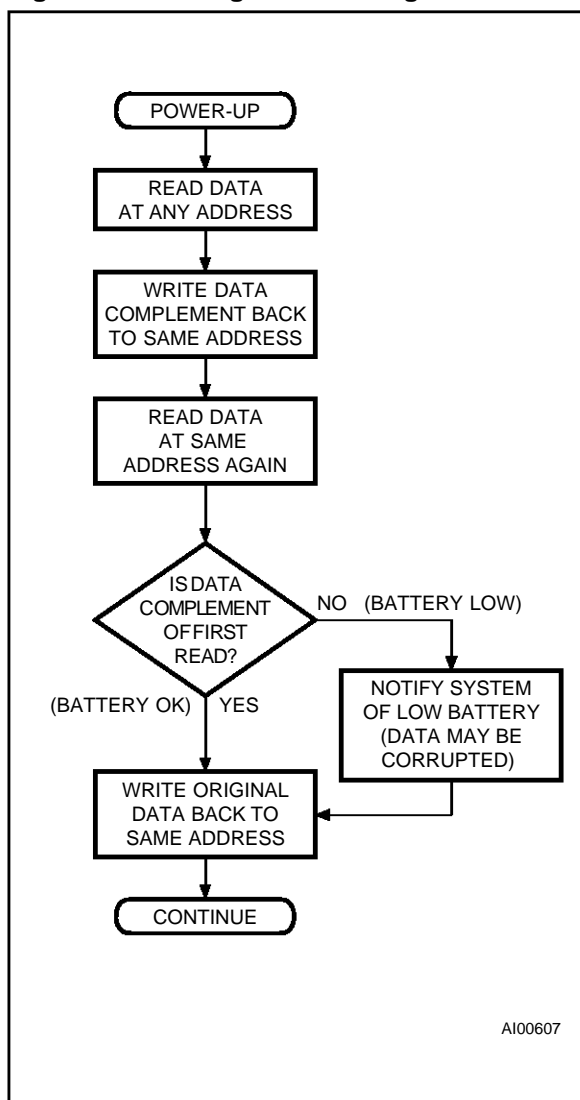
### Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, the seventh bit in the control register. As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0'.

Figure 9. Checking the BOK Flag Status



### Setting the Clock

The eighth bit of the control register is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 10). Resetting the WRITE bit to a '0' then transfers the values of all time registers (7F9h-7FFh) to the actual TIMEKEEPER counters and allows normal operation to resume. The FT bit and the bits marked as '0' in Table 10 must be written to '0' to allow for normal TIMEKEEPER and RAM operation.

### Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T02,12 is shipped from SGS-THOMSON with the STOP bit set to a '1'. When reset to a '0', the M48T02,12 oscillator starts within 1 second.

### Calibrating the Clock

The M48T02,12 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. A typical M48T02,12 is accurate within  $\pm 1$  minute per month at 25°C without calibration. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about  $\pm 1.53$  minutes per month. Of course the oscillation rate of any crystal changes with temperature. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The M48T02,12 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 10. The number of times pulses

are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

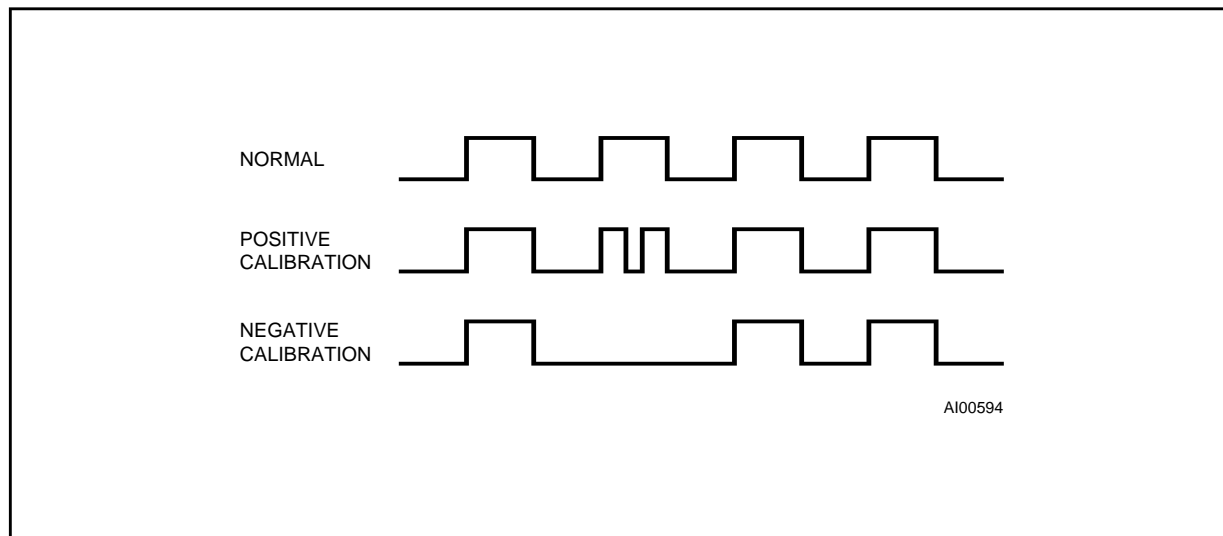
Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month which corresponds to a total range of +5.5 or - 2.75 minutes per month.

**Table 10. Register Map**

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
7FFh	10 Years				Year				Year	00-99
7FEh	0	0	0	10 M.	Month				Month	01-12
7FDh	0	0	10 Date		Date				Date	01-31
7FCh	0	FT	0	0	0	Day			Day	01-07
7FBh	KS	0	10 Hours		Hours				Hour	00-23
7FAh	0	10 Minutes			Minutes				Minutes	00-59
7F9h	ST	10 Seconds			Seconds				Seconds	00-59
7F8h	W	R	S	Calibration					Control	

**Keys:** **S** = SIGN Bit  
**FT** = FREQUENCY TEST Bit (Set to '0' for normal clock operation)  
**KS** = KICK START Bit  
**R** = READ Bit  
**W** = WRITE Bit  
**ST** = STOP Bit  
**0** = Must be set to '0'

Figure 10. Clock Calibration



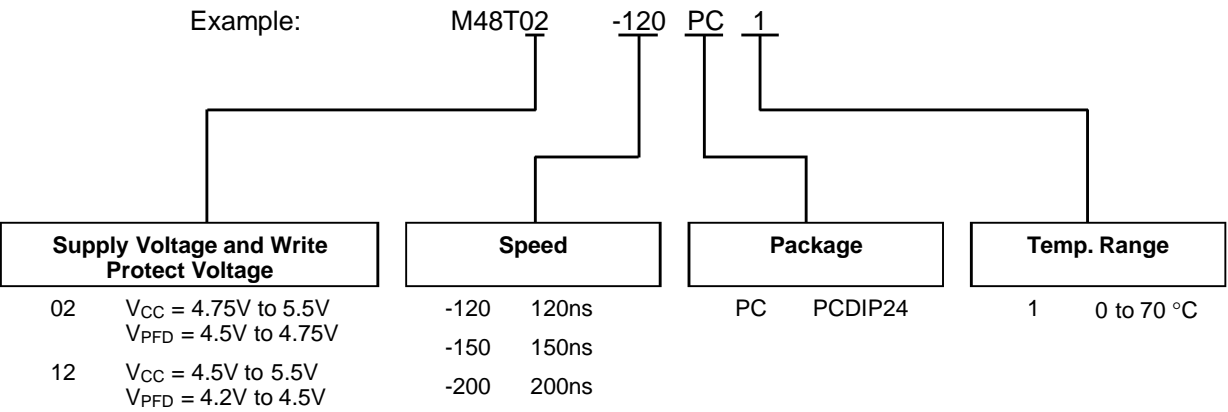
Two methods are available for ascertaining how much calibration a given M48T02,12 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day Register, is set to a '1', and the oscillator is running at 32,768 Hz, the LSB (DQ0) of the Seconds Reg-

ister will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency. The device must be selected and addresses must stable at Address 7F9h when reading the 512 Hz on DQ0.

The FT bit must be set using the same method used to set the clock, using the Write bit. The LSB of the Seconds Register is monitored by holding the M48T02,12 in an extended read of the Seconds Register, without having the Read bit set. The FT bit MUST be reset to '0' for normal clock operations to resume.

ORDERING INFORMATION SCHEME



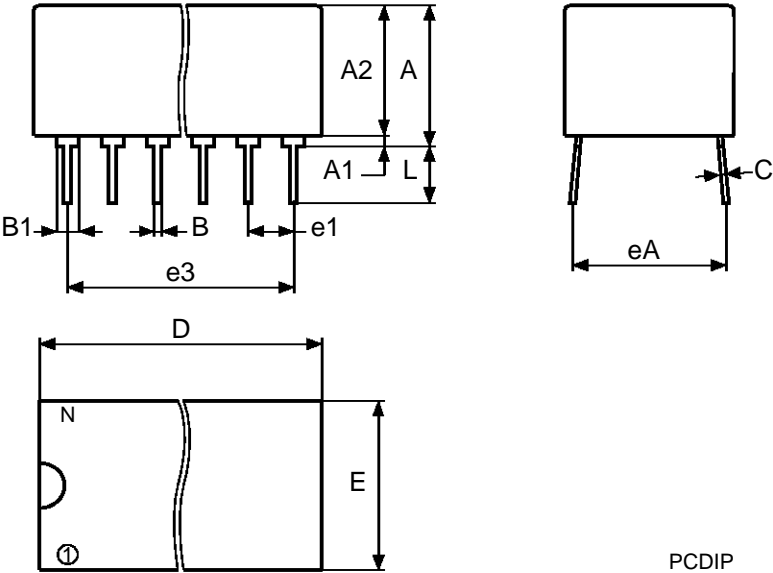
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP24 - 24 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.36	8.89		0.329	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		34.29	34.80		1.350	1.370
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		25.15	30.73		0.990	1.210
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N		24			24	

PCDIP24



PCDIP

Drawing is not to scale

Information furnished is believed to be accurate and reliable. However, SGS-THOMSON Microelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of SGS-THOMSON Microelectronics.

© 1994 SGS-THOMSON Microelectronics - All Rights Reserved

™ TIMEKEEPER, CAPHAT, BYTEWIDE and BiPORT are trademarks of SGS-THOMSON Microelectronics

SGS-THOMSON Microelectronics GROUP OF COMPANIES

Australia - Brazil - China - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco - The Netherlands -  
Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.