

# SN54LS139A, SN54S139, SN74LS139A, SN74S139A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

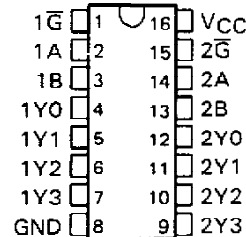
SDLS013

DECEMBER 1972—REVISED MARCH 1988

- Designed Specifically for High-Speed: Memory Decoders  
Data Transmission Systems
- Two Fully Independent 2- to 4-Line Decoders/Demultiplexers
- Schottky Clamped for High Performance

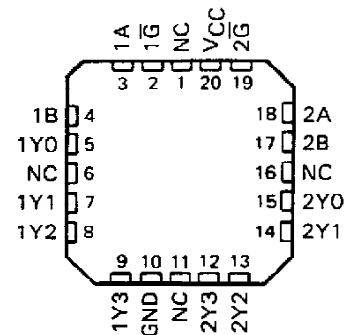
SN54LS139A, SN54S139 ... J OR W PACKAGE  
SN74LS139A, SN74S139A ... D OR N PACKAGE

(TOP VIEW)



SN54LS139A, SN54S139 ... FK PACKAGE

(TOP VIEW)



NC—No internal connection

## description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The circuit comprises two individual two-line to four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

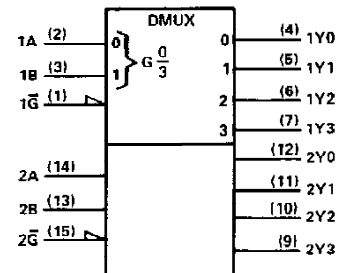
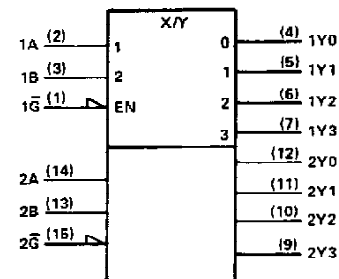
All of these decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and to simplify system design. The SN54LS139A and SN54S139 are characterized for operation range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LS139A and SN74S139A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS		OUTPUTS			
ENABLE	SELECT				
$\overline{\text{G}}$	B A	Y0	Y1	Y2	Y3
H	X X	H	H	H	H
L	L L	L	H	H	H
L	L H	H	L	H	H
L	H L	H	H	L	H
L	H H	H	H	H	L

H = high level, L = low level, X = irrelevant

## logic symbols (alternatives)<sup>†</sup>



<sup>†</sup>These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

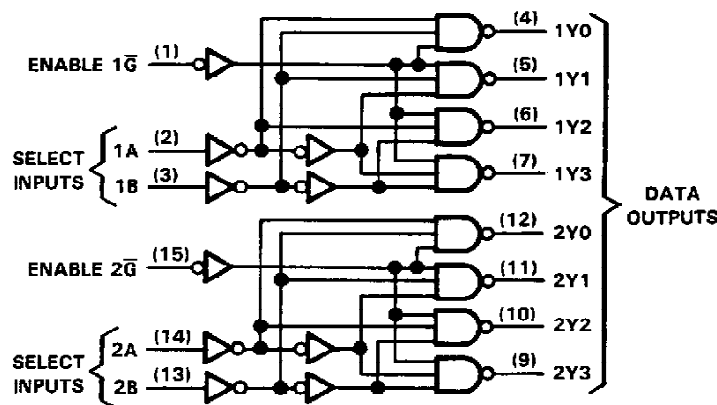
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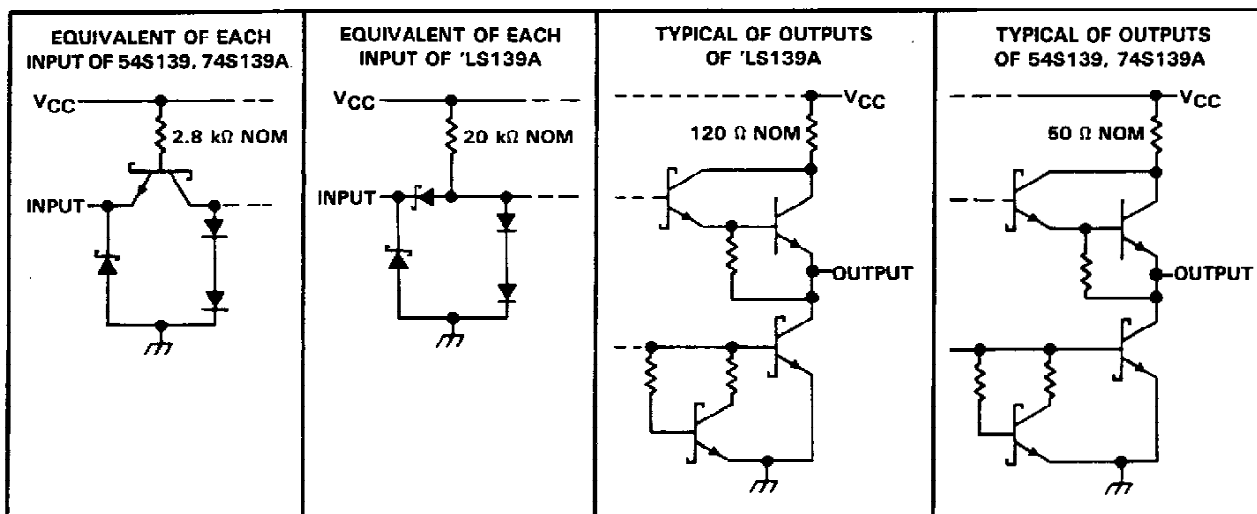
# **SN54LS139A, SN54S139, SN74LS139A, SN74S139A** **DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS**

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

## **schematics of inputs and outputs**



## **absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (See Note 1)	7 V
Input voltage: 'LS139A	7 V
54S139, 74S139A	5.5 V
Operating free-air temperature range: SN54LS139A, SN54S139	-55°C to 125°C
SN74LS139A, SN74S139A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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# SN54LS139A, SN74LS139A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

## recommended operating conditions

		SN54LS139A			SN74LS139A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.7			0.8	V
I <sub>OH</sub>	High-level output current			-0.4			-0.4	mA
I <sub>OL</sub>	Low-level output current			4			8	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS139A		SN74LS139A		UNIT
			MIN	TYP‡ MAX	MIN	TYP‡ MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN,	I <sub>I</sub> = -18 mA	-1.5		-1.5		V
V <sub>OH</sub>	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OH</sub> = -0.4 mA	2.5	3.4	2.7	3.4	V
V <sub>OL</sub>	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX	I <sub>OL</sub> = 4 mA		0.25	0.4	V
			I <sub>OL</sub> = 8 mA		0.35 0.5		
I <sub>I</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 7 V	0.1		0.1		mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.7 V	20		20		μA
I <sub>IL</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0.4 V	-0.4		-0.4		mA
I <sub>OS</sub> §	V <sub>CC</sub> = MAX		-20	-100	-20	-100	mA
I <sub>CC</sub>	V <sub>CC</sub> = MAX,	Outputs enabled and open	6.8 11		6.8 11		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25 °C.

§ Not more than one output should be shorted at a time, and duration of the short circuit test should not exceed one second.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25 °C (see Note 2)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	SN54LS139A SN74LS139A			UNIT
					MIN	TYP	MAX	
t <sub>PLH</sub>	Binary Select	Any	2	R <sub>L</sub> = 2 kΩ,    C <sub>L</sub> = 15 pF		13	20	ns
t <sub>PHL</sub>						22	33	ns
t <sub>PLH</sub>			3			18	29	ns
t <sub>PHL</sub>						25	38	ns
t <sub>PLH</sub>	Enable	Any	2			16	24	ns
t <sub>PHL</sub>						21	32	ns

† t<sub>PLH</sub> = propagation delay time, low-to-high-level output

t<sub>PHL</sub> = propagation delay time, high-to-low-level output

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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# SN54S139, SN74S139A

## DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLIERS

### recommended operating conditions

		SN54S139			SN74S139A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			-1			-1	mA
I <sub>OL</sub>	Low-level output current			20			20	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54S139 SN74S139A			UNIT
			MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA				-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -1 mA	SN54S*	2.5	3.4		V
		SN74S*	2.7	3.4		
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA				0.5	V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V				1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V				50	µA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V				-2	mA
I <sub>OS</sub> §	V <sub>CC</sub> = MAX		-40		-100	mA
I <sub>CC</sub>	V <sub>CC</sub> = MAX, Outputs enabled and open			60	90	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short circuit test should not exceed one second.

### switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Note 2)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	SN54S139 SN74S139A			UNIT	
					MIN	TYP	MAX		
tPLH	Binary Select	Any	2	RL = 280 Ω,      CL = 15 pF		5	7.5	ns	
tPHL						6.5	10	ns	
tPLH			3			7	12	ns	
tPHL						8	12	ns	
tPLH	Enable	Any	2			5	8	ns	
tPHL						6.5	10	ns	

† t<sub>PLH</sub> = propagation delay time, low-to-high-level output

t<sub>PHL</sub> = propagation delay time, high-to-low-level output

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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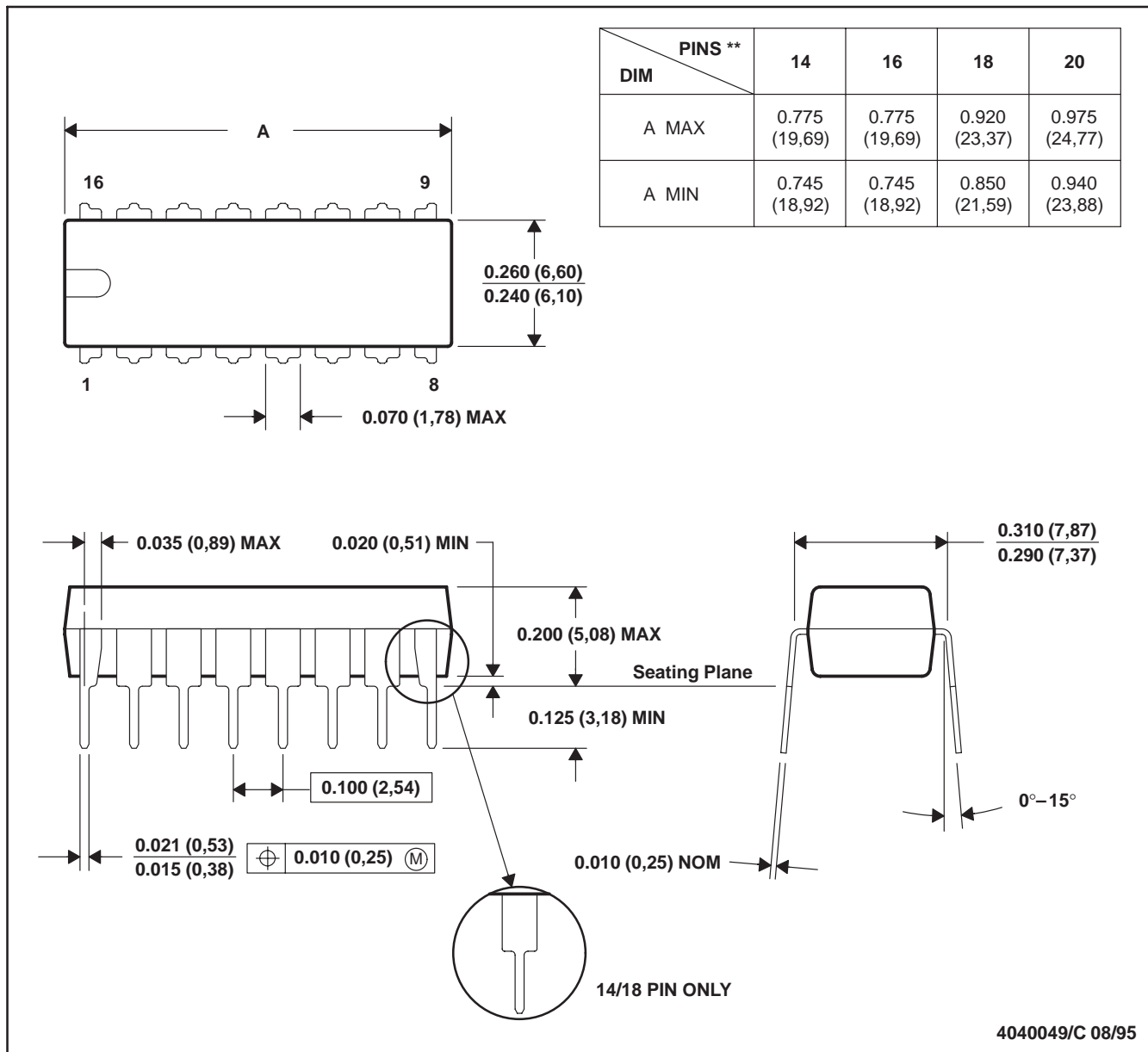
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**N (R-PDIP-T\*\*)****PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).