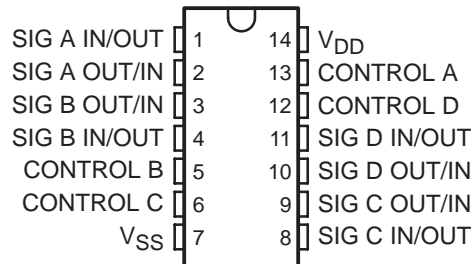


CD4066B CMOS QUAD BILATERAL SWITCH

SCHS051D – NOVEMBER 1998 – REVISED SEPTEMBER 2003

- 15-V Digital or ± 7.5 -V Peak-to-Peak Switching
- 125- Ω Typical On-State Resistance for 15-V Operation
- Switch On-State Resistance Matched to Within 5 Ω Over 15-V Signal-Input Range
- On-State Resistance Flat Over Full Peak-to-Peak Signal Range
- High On/Off Output-Voltage Ratio: 80 dB Typical at $f_{IS} = 10$ kHz, $R_L = 1$ k Ω
- High Degree of Linearity: <0.5% Distortion Typical at $f_{IS} = 1$ kHz, $V_{IS} = 5$ V p-p, $V_{DD} - V_{SS} \geq 10$ V, $R_L = 10$ k Ω
- Extremely Low Off-State Switch Leakage, Resulting in Very Low Offset Current and High Effective Off-State Resistance: 10 pA Typical at $V_{DD} - V_{SS} = 10$ V, $T_A = 25^\circ\text{C}$
- Extremely High Control Input Impedance (Control Circuit Isolated From Signal Circuit): 10¹² Ω Typical
- Low Crosstalk Between Switches: -50 dB Typical at $f_{IS} = 8$ MHz, $R_L = 1$ k Ω
- Matched Control-Input to Signal-Output Capacitance: Reduces Output Signal Transients
- Frequency Response, Switch On = 40 MHz Typical
- 100% Tested for Quiescent Current at 20 V
- 5-V, 10-V, and 15-V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13-B, *Standard Specifications for Description of "B" Series CMOS Devices*
- Applications:
 - Analog Signal Switching/Multiplexing: Signal Gating, Modulator, Squelch Control, Demodulator, Chopper, Commutating Switch
 - Digital Signal Switching/Multiplexing
 - Transmission-Gate Logic Implementation
 - Analog-to-Digital and Digital-to-Analog Conversion
 - Digital Control of Frequency, Impedance, Phase, and Analog-Signal Gain

E, F, M, NS, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The CD4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with the CD4016B, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full signal-input range.

The CD4066B consists of four bilateral switches, each with independent controls. Both the p and the n devices in a given switch are biased on or off simultaneously by the control signal. As shown in Figure 1, the well of the n-channel device on each switch is tied to either the input (when the switch is on) or to V_{SS} (when the switch is off). This configuration eliminates the variation of the switch-transistor threshold voltage with input signal and, thus, keeps the on-state resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage and more constant on-state impedance over the input-signal range. However, for sample-and-hold applications, the CD4016B is recommended.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated

CD4066B CMOS QUAD BILATERAL SWITCH

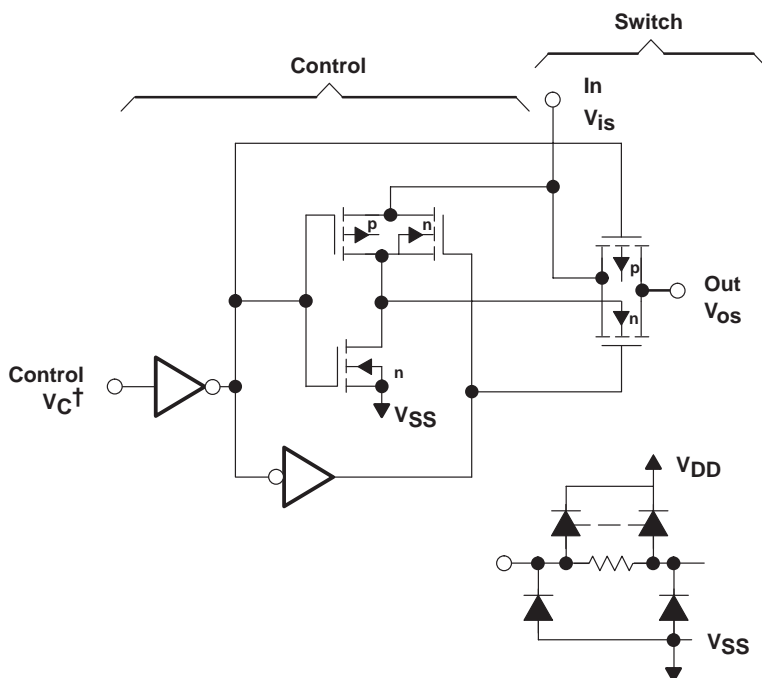
SCHS051D – NOVEMBER 1998 – REVISED SEPTEMBER 2003

description/ordering information (continued)

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	CDIP – F	Tube of 25	CD4066BF3A	CD4066BF3A
	PDIP – E	Tube of 25	CD4066BE	CD4066BE
	SOIC – M	Tube of 50	CD4066BM	CD4066BM
		Reel of 2500	CD4066BM96	
		Reel of 250	CD4066BMT	
	SOP – NS	Reel of 2000	CD4066BNSR	CD4066B
	TSSOP – PW	Tube of 90	CD4066BPW	CM066B
Reel of 2000		CD4066BPWR		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



† All control inputs are protected by the CMOS protection network.

NOTES: A. All p substrates are connected to V_{DD} .

B. Normal operation control-line biasing: switch on (logic 1), $V_C = V_{DD}$; switch off (logic 0), $V_C = V_{SS}$

C. Signal-level range: $V_{SS} \leq V_{is} \leq V_{DD}$

92CS-29113

Figure 1. Schematic Diagram of One-of-Four Identical Switches and Associated Control Circuitry

CD4066B CMOS QUAD BILATERAL SWITCH

SCHS051D – NOVEMBER 1998 – REVISED SEPTEMBER 2003

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

DC supply-voltage range, V_{DD} (voltages referenced to V_{SS} terminal)	–0.5 V to 20 V
Input voltage range, V_{iS} (all inputs)	–0.5 V to $V_{DD} + 0.5$ V
DC input current, I_{iN} (any one input)	±10 mA
Package thermal impedance, θ_{JA} (see Note 1): E package	80°C/W
M package	86°C/W
NS package	76°C/W
PW package	113°C/W
Lead temperature (during soldering):	
At distance $1/16 \pm 1/32$ inch ($1,59 \pm 0,79$ mm) from case for 10 s max	265°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

	MIN	MAX	UNIT
V_{DD} Supply voltage	3	18	V
T_A Operating free-air temperature	–55	125	°C



CD4066B

CMOS QUAD BILATERAL SWITCH

SCHS051D – NOVEMBER 1998 – REVISED SEPTEMBER 2003

electrical characteristics

PARAMETER	TEST CONDITIONS	LIMITS AT INDICATED TEMPERATURES								UNIT
		V _{IN} (V)	V _{DD} (V)	-55°C	-40°C	85°C	125°C	25°C		
								TYP	MAX	
I _{DD} Quiescent device current		0, 5	5	0.25	0.25	7.5	7.5	0.01	0.25	μA
		0, 10	10	0.5	0.5	15	15	0.01	0.5	
		0, 15	15	1	1	30	30	0.01	1	
		0, 20	20	5	5	150	150	0.02	5	
Signal Inputs (V_{IS}) and Outputs (V_{OS})										
r _{on} On-state resistance (max)	V _C = V _{DD} , R _L = 10 kΩ returned to $\frac{(V_{DD} - V_{SS})}{2}$, V _{IS} = V _{SS} to V _{DD}	5		800	850	1200	1300	470	1050	Ω
		10		310	330	500	550	180	400	
		15		200	210	300	320	125	240	
Δr _{on} On-state resistance difference between any two switches	R _L = 10 kΩ, V _C = V _{DD}	5						15		Ω
		10						10		
		15						5		
THD Total harmonic distortion	V _C = V _{DD} = 5 V, V _{SS} = -5 V, V _{IS(p-p)} = 5 V (sine wave centered on 0 V), R _L = 10 kΩ, f _{IS} = 1-kHz sine wave							0.4		%
-3-dB cutoff frequency (switch on)	V _C = V _{DD} = 5 V, V _{SS} = -5 V, V _{IS(p-p)} = 5 V (sine wave centered on 0 V), R _L = 1 kΩ							40		MHz
-50-dB feedthrough frequency (switch off)	V _C = V _{SS} = -5 V, V _{IS(p-p)} = 5 V (sine wave centered on 0 V), R _L = 1 kΩ							1		MHz
I _{IS} Input/output leakage current (switch off) (max)	V _C = 0 V, V _{IS} = 18 V, V _{OS} = 0 V; and V _C = 0 V, V _{IS} = 0 V, V _{OS} = 18 V	18		±0.1	±0.1	±1	±1	±10 ⁻⁵	±0.1	μA
-50-dB crosstalk frequency	V _{C(A)} = V _{DD} = 5 V, V _{C(B)} = V _{SS} = -5 V, V _{IS(A)} = 5 V _{p-p} , 50-Ω source, R _L = 1 kΩ							8		MHz
t _{pd} Propagation delay (signal input to signal output)	R _L = 200 kΩ, V _C = V _{DD} , V _{SS} = GND, C _L = 50 pF, V _{IS} = 10 V (square wave centered on 5 V), t _r , t _f = 20 ns	5						20	40	ns
		10						10	20	
		15						7	15	
C _{IS} Input capacitance	V _{DD} = 5 V, V _C = V _{SS} = -5 V							8		pF
C _{OS} Output capacitance	V _{DD} = 5 V, V _C = V _{SS} = -5 V							8		pF
C _{IOS} Feedthrough	V _{DD} = 5 V, V _C = V _{SS} = -5 V							0.5		pF



electrical characteristics (continued)

CHARACTERISTIC	TEST CONDITIONS	LIMITS AT INDICATED TEMPERATURES						UNIT	
		V _{DD} (V)	-55°C	-40°C	85°C	125°C	25°C		
							TYP	MAX	
Control (V_C)									
V _{I(LC)} Control input, low voltage (max)	I _{is} < 10 μA, V _{is} = V _{SS} , V _{OS} = V _{DD} , and V _{is} = V _{DD} , V _{OS} = V _{SS}	5	1	1	1	1	1	1	V
		10	2	2	2	2	2	2	
		15	2	2	2	2	2	2	
V _{I(HC)} Control input, high voltage	See Figure 6	5	3.5 (MIN)						V
		10	7 (MIN)						
		15	11 (MIN)						
I _{IN} Input current (max)	V _{is} ≤ V _{DD} , V _{DD} - V _{SS} = 18 V, V _{CC} ≤ V _{DD} - V _{SS}	18	±0.1	±0.1	±1	±1	±10 ⁻⁵	±0.1	μA
Crosstalk (control input to signal output)	V _C = 10 V (square wave), t _r , t _f = 20 ns, R _L = 10 kΩ	10					50		mV
Turn-on and turn-off propagation delay	V _{IN} = V _{DD} , t _r , t _f = 20 ns, C _L = 50 pF, R _L = 1 kΩ	5					35	70	ns
		10					20	40	
		15					15	30	
Maximum control input repetition rate	V _{is} = V _{DD} , V _{SS} = GND, R _L = 1 kΩ to GND, C _L = 50 pF, V _C = 10 V (square wave centered on 5 V), t _r , t _f = 20 ns, V _{OS} = 1/2 V _{OS} at 1 kHz	5					6		MHz
		10					9		
		15					9.5		
C _I Input capacitance							5	7.5	pF

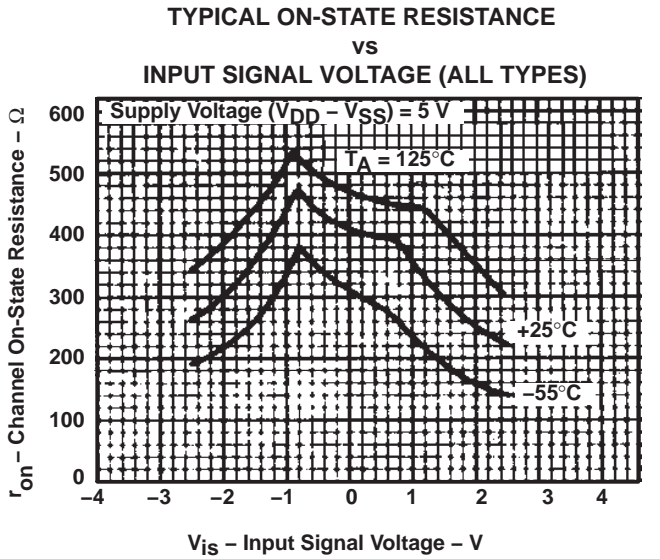
switching characteristics

V _{DD} (V)	SWITCH INPUT						SWITCH OUTPUT, V _{OS} (V)	
	V _{is} (V)	I _{is} (mA)					MIN	MAX
		-55°C	-40°C	25°C	85°C	125°C		
5	0	0.64	0.61	0.51	0.42	0.36	0.4	
5	5	-0.64	-0.61	-0.51	-0.42	-0.36	4.6	
10	0	1.6	1.5	1.3	1.1	0.9	0.5	
10	10	-1.6	-1.5	-1.3	-1.1	-0.9	9.5	
15	0	4.2	4	3.4	2.8	2.4	1.5	
15	15	-4.2	-4	-3.4	-2.8	-2.4	13.5	

CD4066B CMOS QUAD BILATERAL SWITCH

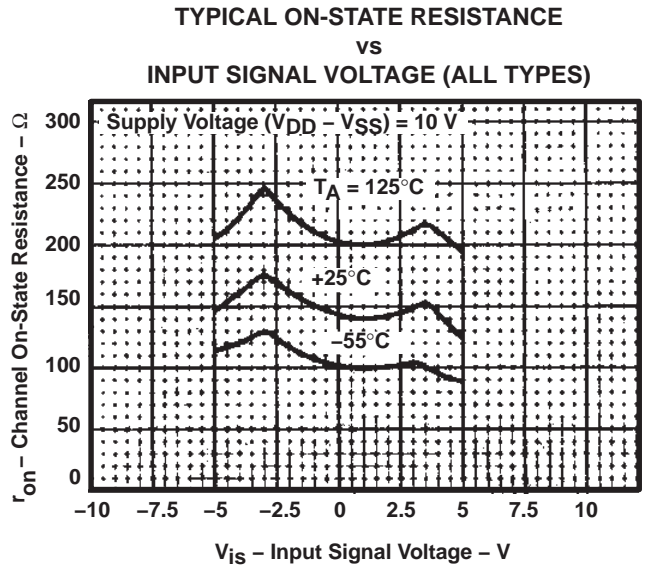
SCHS051D – NOVEMBER 1998 – REVISED SEPTEMBER 2003

TYPICAL CHARACTERISTICS



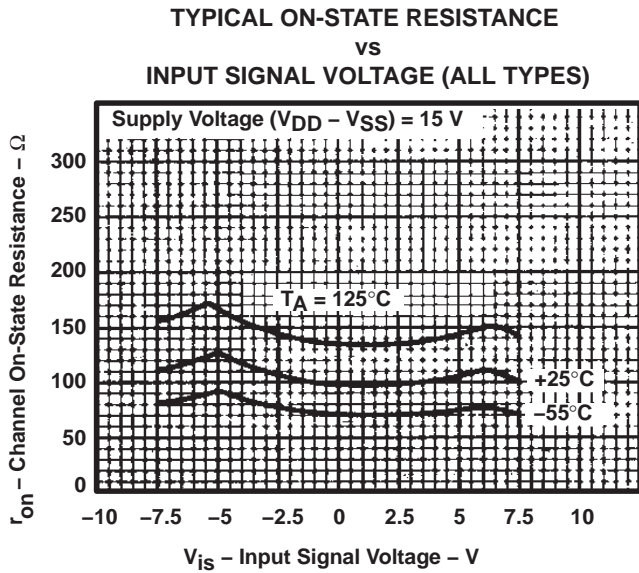
92CS-27326RI

Figure 2



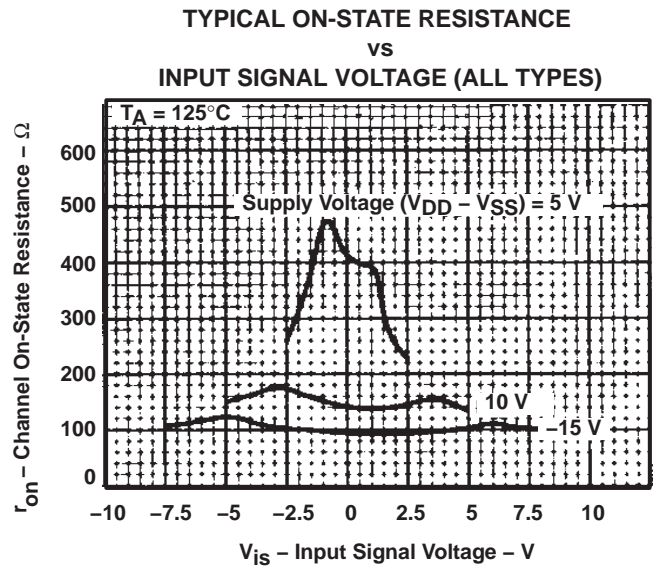
92CS-27327RI

Figure 3



92CS-27329RI

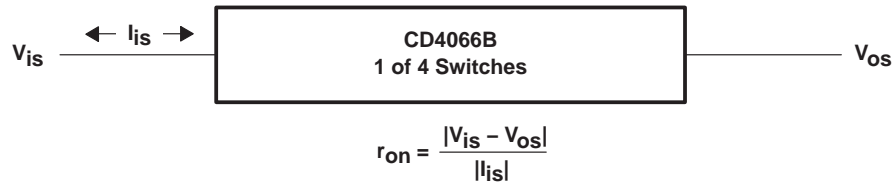
Figure 4



92CS-27330RI

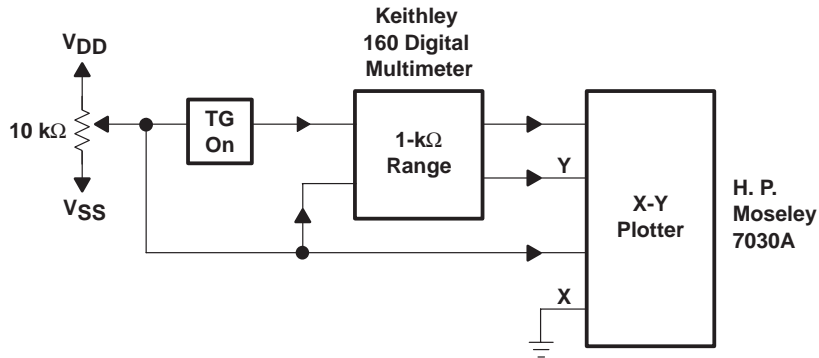
Figure 5

TYPICAL CHARACTERISTICS



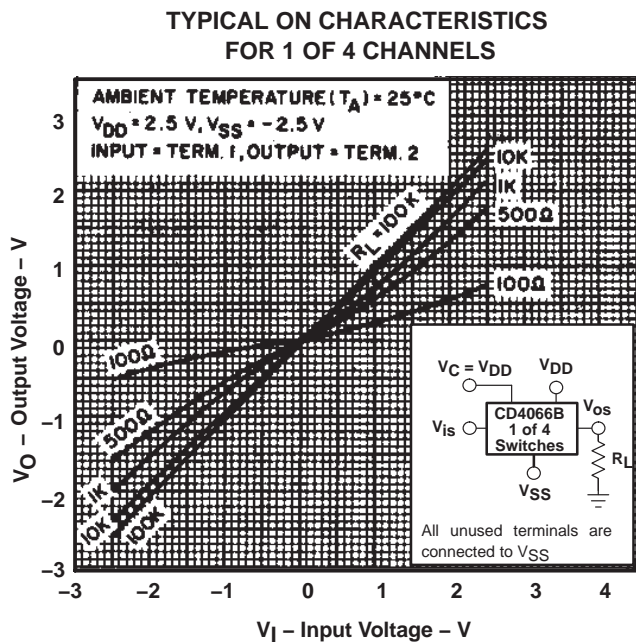
92CS-30966

Figure 6. Determination of r_{on} as a Test Condition for Control-Input High-Voltage (V_{IHC}) Specification



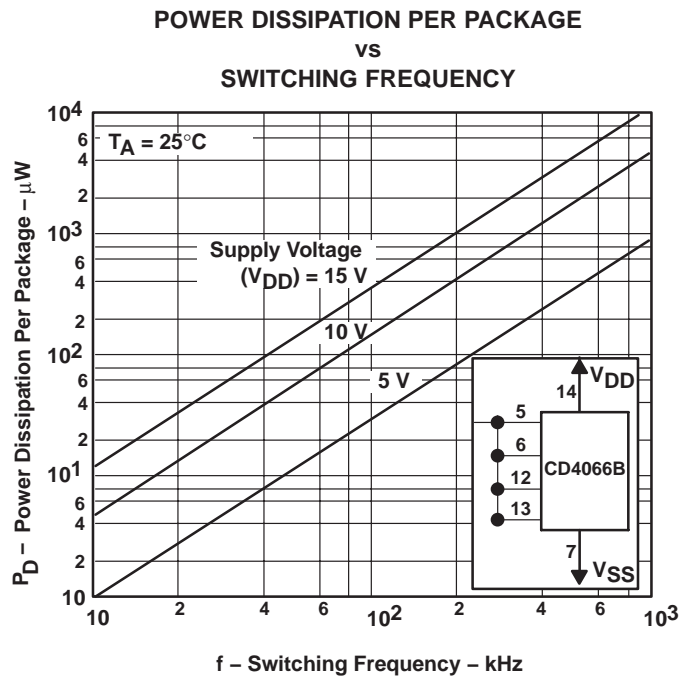
92CS-22716

Figure 7. Channel On-State Resistance Measurement Circuit



92CS-30919

Figure 8



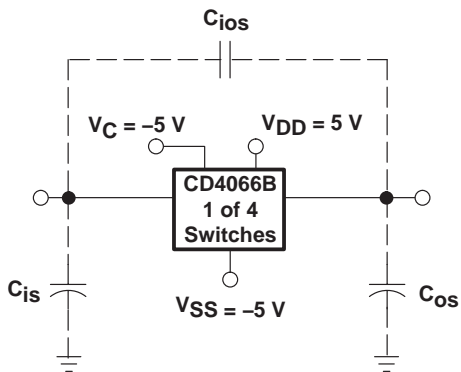
92CS-30920

Figure 9

CD4066B CMOS QUAD BILATERAL SWITCH

SCHS051D – NOVEMBER 1998 – REVISED SEPTEMBER 2003

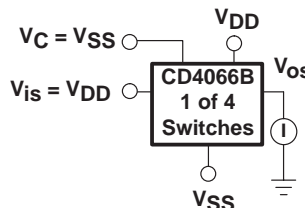
TYPICAL CHARACTERISTICS



92CS-30921

Measured on Boonton capacitance bridge, model 75a (1 MHz); test-fixture capacitance nulled out.

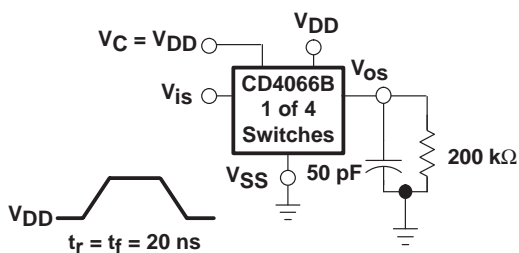
Figure 10. Typical On Characteristics for One of Four Channels



92CS-30922

All unused terminals are connected to V_{SS} .

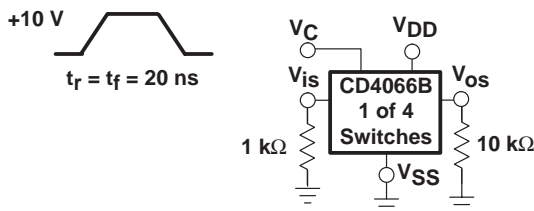
Figure 11. Off-Switch Input or Output Leakage



92CS-30923

All unused terminals are connected to V_{SS} .

Figure 12. Propagation Delay Time Signal Input (V_{is}) to Signal Output (V_{os})

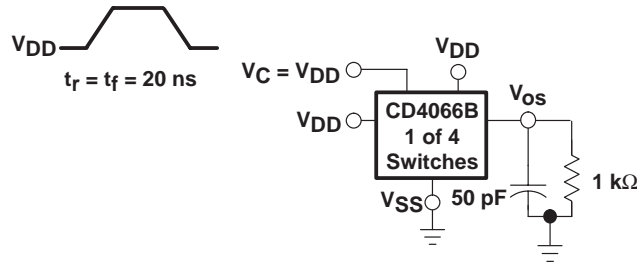


92CS-30924

All unused terminals are connected to V_{SS} .

Figure 13. Crosstalk-Control Input to Signal Output

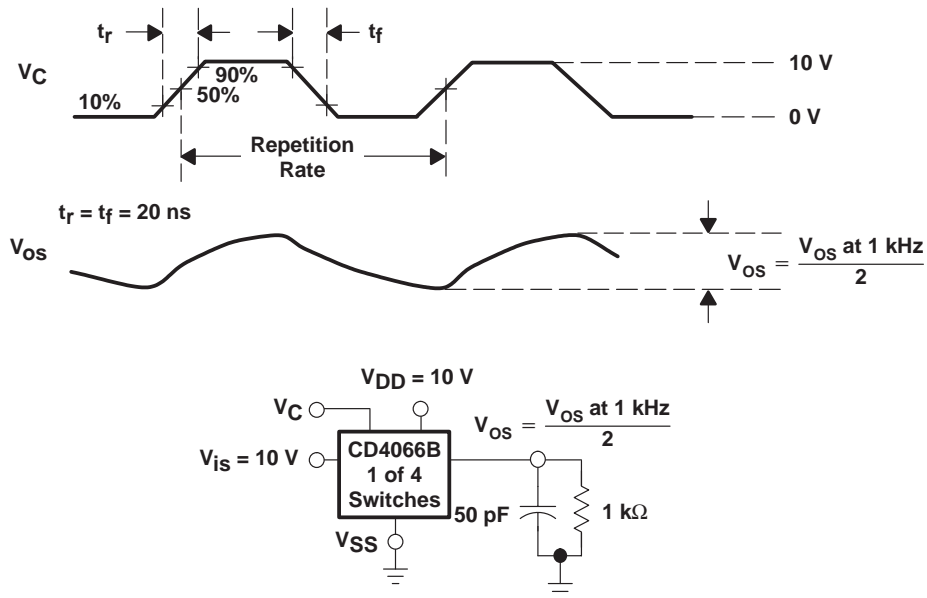
TYPICAL CHARACTERISTICS



- NOTES: A. All unused terminals are connected to V_{SS} .
B. Delay is measured at V_{OS} level of +10% from ground (turn-on) or on-state output level (turn-off).

92CS-30925

Figure 14. Propagation Delay, t_{PLH} , t_{PHL} Control-Signal Output



All unused terminals are connected to V_{SS} .

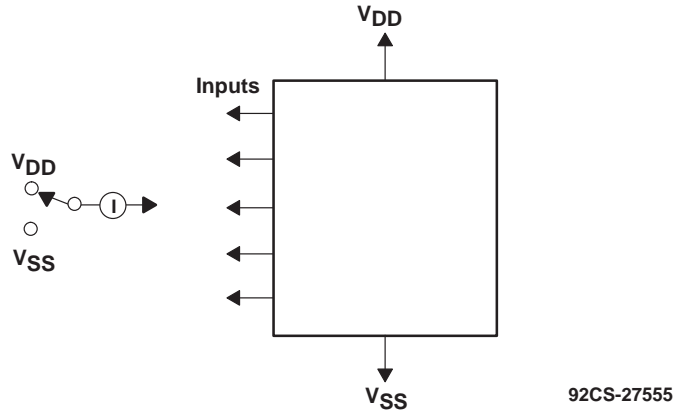
92CS-30925

Figure 15. Maximum Allowable Control-Input Repetition Rate

CD4066B CMOS QUAD BILATERAL SWITCH

SCHS051D – NOVEMBER 1998 – REVISED SEPTEMBER 2003

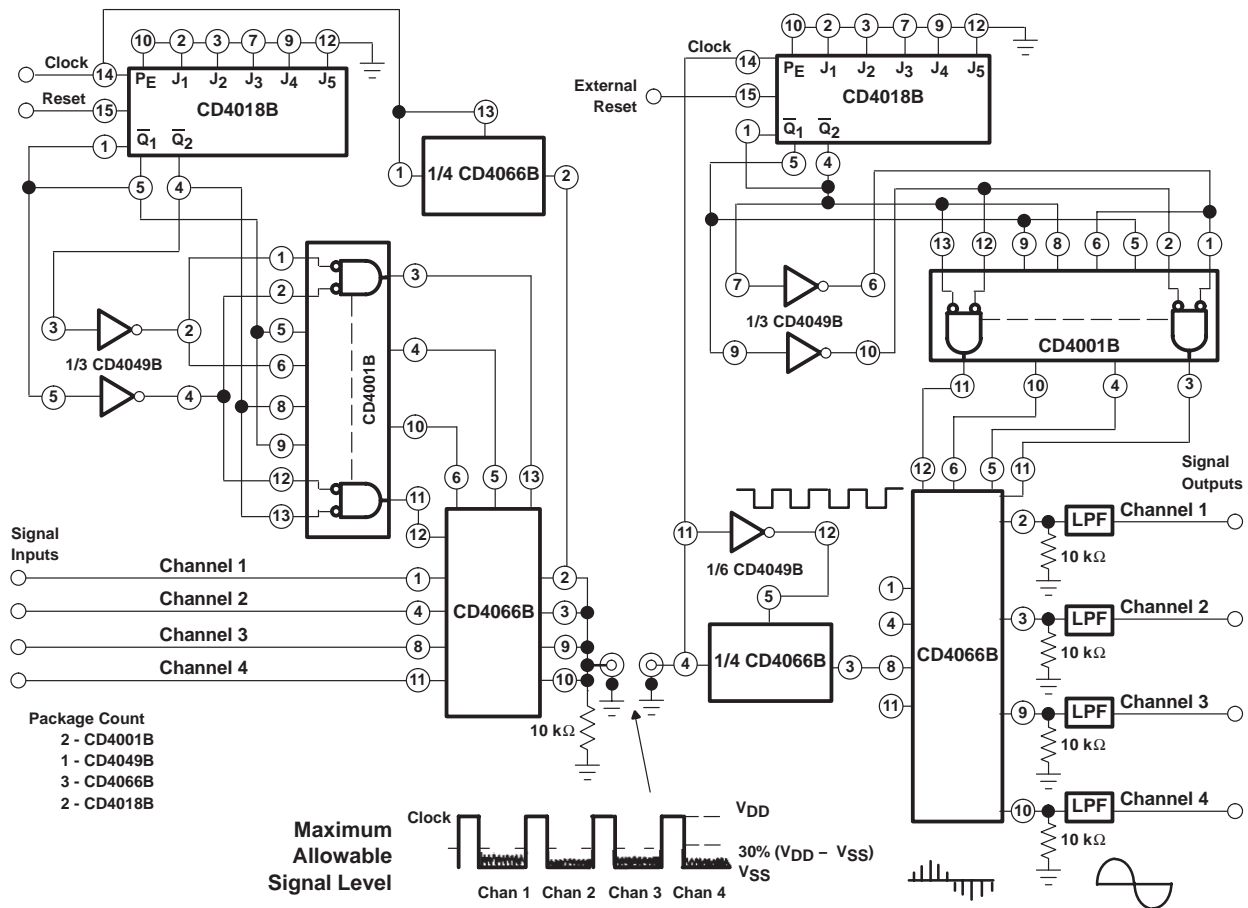
TYPICAL CHARACTERISTICS



92CS-27555

Measure inputs sequentially to both V_{DD} and V_{SS} . Connect all unused inputs to either V_{DD} or V_{SS} . Measure control inputs only.

Figure 16. Input Leakage-Current Test Circuit



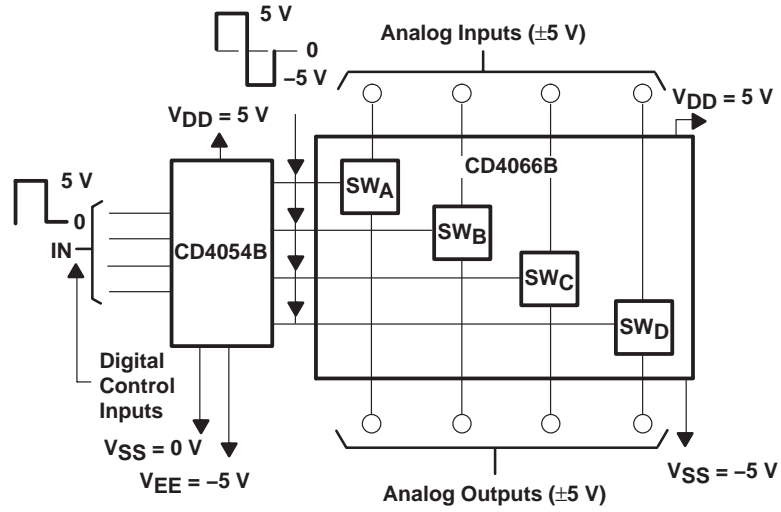
92CM-30928

Figure 17. Four-Channel PAM Multiplex System Diagram



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS



92CS-30927

Figure 18. Bidirectional Signal Transmission Via Digital Control Logic

CD4066B

CMOS QUAD BILATERAL SWITCH

SCHS051D – NOVEMBER 1998 – REVISED SEPTEMBER 2003

APPLICATION INFORMATION

In applications that employ separate power sources to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the four CD4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4066B.

In certain applications, the external load-resistor current can include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 V (calculated from r_{on} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4066BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4066BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4066BF	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4066BF3A	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4066BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4066BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
JM38510/05852BCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

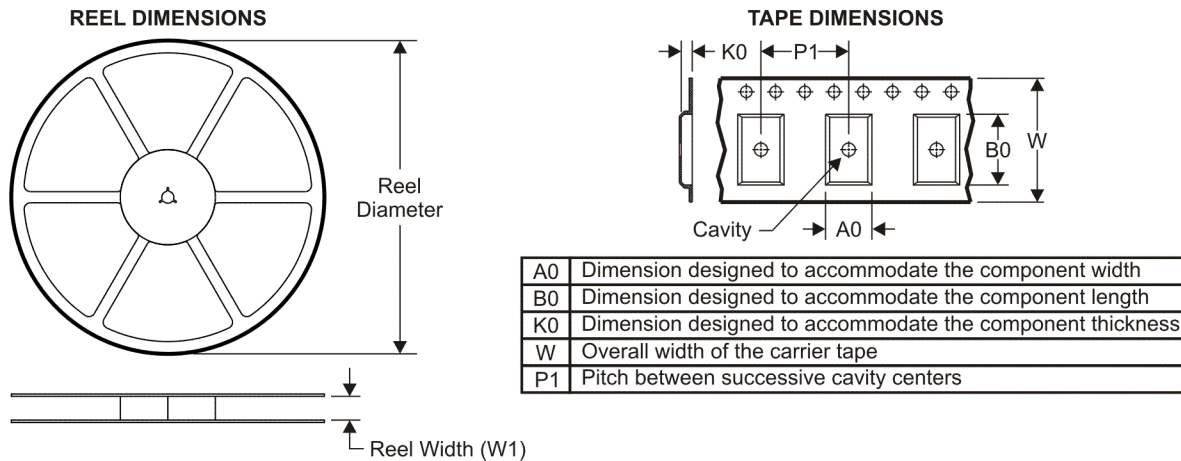
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4066BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4066BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4066BPWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4066BM96	SOIC	D	14	2500	333.2	345.9	28.6
CD4066BM96	SOIC	D	14	2500	346.0	346.0	33.0
CD4066BNSR	SO	NS	14	2000	346.0	346.0	33.0
CD4066BPWR	TSSOP	PW	14	2000	346.0	346.0	29.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-3/H 11/2006

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated